Band gap engineering of the ZnO/Si heterojunction using amorphous buffer layers

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ABSTRACT

Zinc oxide is attractive for photovoltaic applications due to its properties as Transparent Conductive Oxide (TCO), as well as for rectifying heterojunctions to silicon. The present work investigates the electrical properties of the ZnO/Si heterojunction and the influence of buffer layers; i.e. ZnO/buffer/Si structures. The structures have been produced with buffer thicknesses in the range $5 - 20\ nm$, composed of amorphous silicon (aSi), silicon germanium (aSiGe) or silicon carbide (aSiC). The compositional variation is done to alter the band gap of the buffer layer; approximately $1.9\ eV$ was anticipated for aSi and the addition of Ge should decrease this value while an increase is expected from C. The deposition techniques Plasma Enhanced Chemical Vapor Deposition (PECVD) and sputter deposition was used for synthesis, and characterization has primarily been focused on electrical characteristics. Current-Voltage (IV) characteristics show high rectification for most samples, and an improvement is observed for the structures with a buffer layer compared to the samples without buffer layer on p-type substrates. Both IV and Capacitance-Voltage (CV) measurements indicate deviations from thermionic emission theory and the Schottky-Mott model, which is further elaborated on by studying the temperature dependence of these measurements. These deviations in IV and CV data are supported by broad peaks observed in Deep Level Transient Spectroscopy (DLTS) spectra, indicating distributions of defects throughout the band gap. Fermi level pinning is discussed as an explanation for the high barrier heights derived from the IV measurements. Accompanying this, inhomogeneity in the junction properties is considered to explain the difference in the IV and CV results, as well as temperature dependences of these. Finally, as a proof of concept, the samples has been investigated for photovoltaic effect in a solar simulator.

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PART I - THEORY

1 INTRODUCTION

In the recent publication from the Intergovernmental Panel on Climate Change (IPCC) [1], the increase of scientific confidence in the existence and causes of anthropogenic climate change is documented. It is concluded that "*It is extremely likely that human influence has been the dominant cause of the observed warming since the mid-20th century*", and further, that *"The largest contribution … is caused by the increase in the atmospheric concentration of* CO_2*"*. With the 2009 UN Climate Change Conference in Copenhagen an agreement was reached that the warming should be limited to 2 ℃ from pre-industrial level. Today the warming has already reached 0.8 ℃, and in 2012 the annual global emission of CO_2 increased with 1.4 % reflecting a still increasing demand for energy. In the World Energy Outlook of 2013 the International Energy Agency (IEA) suggests that the trend of increasing emission must be turned within 2020 for a modest 50 % chance of reaching the 2 ℃ goal. [2]

The crux of the situation is to achieve reduction of emission while simultaneously accommodating population growth and pulling millions of people in developing countries out of poverty. This is an extremely challenging task that calls for vast technological change in a historically short time frame. Technology development for renewable energy production is central to disengage from the dependence on fossils. In this respect solar energy from photovoltaics (PV) should play an important role. PV is still a minor player in the global electricity production, with only 0.4 %, but a tremendous development has been seen in installed capacity over the last decade. In 2013 the total installed capacity reached 136 GW, 52 times that of 2003 and a 36 % increase from 2012 [3]. The foundation for the market has been the governmental incentives in central European countries, with Germany in the lead. Recently, the rapid development can also be attributed to Chinese subsidies of production. These subsidies have since 2008 resulted in overproduction, with subsequent dumping of module prices and widespread financial crisis in the industry[4, 5]. Those pulling through have done so by optimizing the production to minimize cost. With few exceptions the consumers are, however, still depending on government incentives to come close to grid parity in terms of power cost. This calls for further development of the technologies in terms of reduced production cost or higher module efficiency.

Silicon based solar cells dominate the market, but with competition from a variety of different thin-film technologies. In addition to traditional silicon cells with pn-junction of differently doped regions, significant market shares have recently been claimed by the so called HIT structure. HIT abbreviate Heterojunction with Intrinsic Thin layer, and is a structure initially developed by Sanyo. Panasonic, who bought Sanyo in 2009, further developed the structure and in April 2014 announced a record 25.6 % efficiency, thus surpassing the record for traditional mono-crystalline silicon (mc-Si) [6]. The HIT structure is based on mc-Si wafers, but utilize amorphous silicon (aSi) as an intrinsic layer and

emitter. Transparent Conductive Oxides (TCO) are used on the HIT structure to reduce the loss from shading from traditional metal front side contacts. As TCO, Indium Tin Oxide (ITO) is commonly used for its high conductivity and transparency to visible light. ITO is, however, expected to be increasingly expensive due to indium scarcity, and other materials are needed. In this respect, zinc oxide (ZnO) has become a promising alternative, and with higher abundance it is deemed to have a higher commercial potential.

ZnO is a semiconductor with a wide and direct band gap of $3.37\ eV$, thus transparent to visible light. With the ability to be doped degenerately, high conductivity is achievable, and combining these two properties makes it interesting as a TCO. For ZnO to come on par with ITO in terms of performance, continued investigations must be made on its synthesis. Of particular interest are the interface properties to silicon. The ZnO/Si heterojunction is also found to be rectifying, and thus have potential for photovoltaic action on its own. This is, however, challenged by lattice mismatch of the two materials and band alignment, which gives high recombination rates for charge carriers. Knutsen et al. [7] discuss alloying the ZnO with magnesium (Mg) to engineer the band gap and improve on the recombination rates. Their simulation results indicate the possibility of solar cells with efficiency exceeding 20 %. An alternative approach is to do the band gap engineering on the Si side of the junction, and this sets the stage for the work done in this thesis.

The present work reports on a study of the ZnO/Si heterojunction, and by introducing an amorphous buffer layer, giving the HIT-like structure ZNO/buffer/Si. The intention of the buffer layer is to alter the band structure in the junction, and possibly change the interface properties with respect to defects. With aSi as the starting point, the buffers have also been made with additions of germanium (aSiGe) to decrease the band gap, and carbon (aSiC) to increase it. These structures were synthesized on n-type and p-type mono-crystalline wafers. aSi films are normally realized using Plasma Enhanced Chemical Vapor Deposition (PECVD), but in order to introduce Ge and C magnetron sputter deposition has been employed as well. Aluminum doped ZnO (AZO) films were fabricated with magnetron sputter deposition. The main focus has been on electrical characterization of the structures with current-voltage (IV), capacitance-voltage (CV) and Deep Level Transient Spectroscopy (DLTS). From IV and CV, figures of merit such as rectification, ideality factor and barrier height have been evaluated. This has been compared to the defect studies of the interface performed with DLTS, and conduction mechanisms and interface properties are discussed. Structural and optical properties have also been investigated through transmission measurements of UV and visible light, Hall effect and X-ray diffraction experiments.

The contents of this thesis are divided in three parts. The present chapter is contained in part I, and so is the next chapter, giving the theoretical background for the experimental work. Part II holds chapters 3 through 6, and focus on experimental methods. This includes synthesis methods, sample preparation and characterization methods. Some simulations have also been done, and the methodic for these are also included in part II. In part III the results are presented and discussed in chapter 7, followed by summarization and concluding remarks in chapter 8.

2 BACKGROUND

The purpose of this chapter is to give an overview of the basic theory relevant to the work reported in this thesis. The chapter will start with a short introduction to crystallography and defects. Properties of semiconducting materials and devices will follow, leading to a discussion of their application in photovoltaics. Finally, previous work on the relevant materials will be reviewed in the last section.

2.1 STRUCTURE OF SOLIDS

The following account of solid state physics in this and the next section is given based on reviews in textbooks by Tilley [8], Hemmer [9] and Kittel [10].

Crystallography is the study of crystalline materials. Prior to the development of sophisticated methods for studies of atomic structures, these materials were characterized by angles and planes on the macroscopic level. With the development of diffraction methods, using radiation with x-rays, electrons and neutrons, it became possible to relate the macroscopic symmetries to the microscopic ordering of atoms. It is interference from reflections of the radiation from layers of atoms that gives diffraction, and the result is patterns revealing the prominent planes. These patterns act as fingerprints identifying the underlying structure. With diffraction techniques came also the understanding of poly-crystalline materials, that is, materials composed of crystallite grains with different orientations.

To describe a crystal structure it is reasonable to divide the crystal into the smallest piece that can be used to replicate the whole structure. This small piece is called the primitive unit cell and consists of a basis of an atom or a molecule, and translation vectors representing the repeating lattice. Seven different lattice systems exist based on different angles and length ratios between the unit vectors. From these the total of 14 Bravais lattices is defined by adding additional points in the center of, or on the faces of the volume spanned by the unit vectors. Larger, non-primitive, unit cells are frequently used for ease of visualization, although the underlying symmetries and relations are kept.

For many materials the most energetically favorable ordering is a close packing of the atoms. Considering the atoms as hard spheres helps the understanding. For a material with only one kind of atoms the highest density is achieved if each sphere has six nearest neighbors in the plane, and 12 in three dimensions. Stacking of planes enables two configurations of this kind; these are named the Face Centered Cubic (FCC) structure and the Hexagonal Close Packed (HCP) structure in the Bravais system.

Silicon crystalizes in the so called diamond structure. This is an FCC structure with a diatomic basis where the atoms on the lattice points are accompanied by atoms displaced with a vector [¼ ¼ ¼] from each lattice point. Notice that with this basis the atoms are no longer close packed; energy considerations are also determined by valence, and the tetrahedral coordination in this structure is suitable for silicon.

A close relative to the diamond structure is the zinc blende structure, named after the mineral ZnS. Here a molecule of two different atoms are separated the same way as the two silicon atoms in the diamond structure. Tetrahedral coordination results for both atom types. A similar tetrahedral orientation of molecules with two atoms is achievable in the HCP structure known as wurtzite. Zinc oxide adopts the wurtzite structure under the conditions relevant to this work.

Also important to this work are materials without crystal structure, i.e. amorphous materials. Looking at amorphous silicon, abbreviated aSi, at a microscopic level reveals a tetrahedral coordination much like the crystalline version. However, the long range ordering is disturbed by slight deviations in the angle of the bonds and some bonds are left unfulfilled, called dangling bonds. Planes and directions as in the crystalline counterpart are not present and diffraction analysis leads to smeared out results rather than clear patterns.

2.2 CRYSTAL DEFECTS

In the previous section, the idealized structures of crystalline materials were described. This perfect periodicity is easy to handle, and a good start when characterizing materials. However, it turns out that many important characteristics are related to deviations in this structure, collectively called defects.

It is common to categorize defects from their dimensionality in the material. A three dimensional defect extends in all directions and can be a precipitate of a foreign material, a different phase or even a cavity. Stacking faults and grain boundaries are examples of two dimensional defects. A stacking fault is a disruption in the repeating sequence of layers of atoms. Grain boundaries separate the crystallites and are inevitable in all multi-crystalline materials. One dimensional defects or line defects can be exemplified by dislocations and are a common result from strain in a material.

Zero dimensional defects are commonly called point defects and are particularly important in the context of this work. This is because they are often associated with an electrical charge and thus influence the electrical properties of the system. In the following, the term defects will predominantly refer to point defects. Several different point defects are possible and some of these are depicted in Figure 1. A separation is made between intrinsic and extrinsic defects, explained in the following subsections.

INTRINSIC DEFECTS

Intrinsic defects are native to a material and exist also in stoichiometric and pure materials. Self-interstitials and vacancies are examples of such defects, and their concentration depends on thermodynamic considerations. The equilibrium concentrations are given by minimization of Gibbs free energy G. This is a balance between enthalpy of formation of the defect H, and the configurational entropy associated with the defect distribution S:

$$G = H - TS \tag{2.1}$$

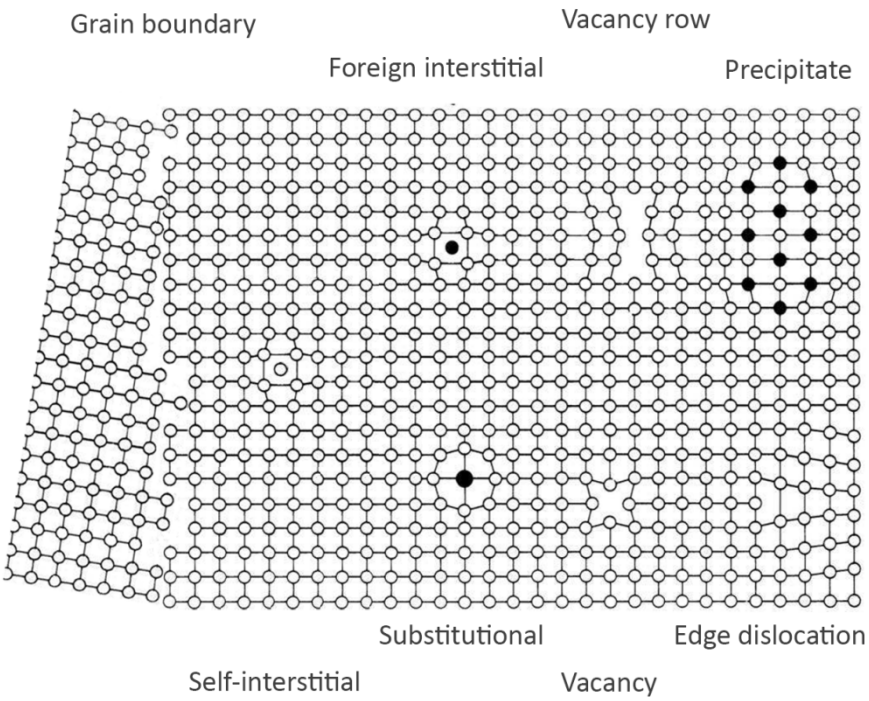

Figure 1 - The important point defects are shown in this figure. So is also the one dimensional vacancy row and edge dislocation, a two dimensional grain boundary, and a three dimensional foreign precipitate. The figure is adapted from Almar-Næss [11].

From the entropy term follows also the temperature dependence which is characteristic for the concentration of intrinsic defects.

If the defects are associated with an electric charge, electroneutrality considerations require equal concentrations of positive and negative defects. This is especially relevant in materials with ionic properties. A Schottky defect pair, which is a pair of vacancies of different charge, exemplifies this:

$$0 \Leftrightarrow v_{Zn}^{//} + v_{O}^{\bullet\bullet}$$

Here ZnO is used as the example and the v's denote a vacancy on the site described by their subscript. The superscripts / and • describe negative and positive effective charge relative to the site without a defect, respectively. An x would be used in the case of a neutral defect. This nomenclature is known as Kröger-Vink, and described in detail elsewhere [12]. The equation is written as a chemical reaction where the 0 represent the perfect structure before the defects were generated.

Another possible pairing of intrinsic defects is known as a Frenkel pair. This consists of a vacancy and an interstitial of the same element. Generally both Schottky and Frenkel pairs exist, but different materials are dominated by one or the other depending on several factors such as packing density and size ratio between cations and anions in ionic materials.

EXTRINSIC

Extrinsic defects occur as substitutional atoms or foreign interstitials, as shown in Figure 1, and can be present in a material up to the solid solubility limit when the material is in thermal equilibrium. At higher concentrations precipitation of a secondary phase is more thermodynamically favorable, although it is possible to freeze in defects by e.g. a rapid cooling process.

As for intrinsic defects, a substitutional atom with valence differing from the host site obtains an effective charge which must be compensated for charge neutrality. The compensation can come from any defect of opposite charge, whether intrinsic or extrinsic. By intentionally introducing foreign elements that are compensated with electronic defects the electrical properties of the material can be altered. This is called doping, and even trace amounts of the dopants can significantly change the conductivity. The mechanism and effect of doping is considered in section 2.3.2.

2.3 SEMICONDUCTOR PHYSICS

Solid materials are commonly divided in three categories; metals, semiconductors and insulators, the division coming from their ability to conduct electrical current. Semiconductors are especially important because junctions of different materials are the foundation for transistors and diodes, and thus almost all modern electronics, as well as solar cells which is relevant here. To understand the electrical properties of semiconductors, and how they separate from metals and insulators one must consider the fundamentals of electronic states in atoms. Crystalline structures will be used as example, while key differences in amorphous semiconductors are summarized in section 2.3.3. This review is based on the textbook by Streetman et al. [13].

2.3.1 ENERGY BANDS

When a large number of atoms come together to form a crystalline solid, the discrete electronic states of the single atoms combine into what is called energy bands. Energy bands are continuous regions on the energy scale that is available to electrons. These bands result from the overlapping of quantum mechanical wave functions for the individual electrons and are separated by regions that cannot be occupied. The regions without available states are called band gaps. The extent of the overlapping of the wave functions depends on the crystal structure and its periodicity. Mathematical description of this periodicity is done in reciprocal space. Here the unit vectors have lengths inversely proportional to the interatomic spacing and directions normal to the lattice planes. A vector $\boldsymbol{k}$ in reciprocal space is thus a wave vector and proportional to the crystal momentum. Then a dispersion relation $E_n(\boldsymbol{k})$ for each band n can be calculated, and the representation of all bands in the reciprocal space amounts to the band structure of the material. It is common to present this by choosing a selection of points in the reciprocal space corresponding to important crystal directions and plot the energy as function of $\boldsymbol{k}$ two-dimensionally between these. This is shown in Figure 2a and b for silicon and zinc oxide, respectively. A simplified representation of the band diagram is shown in Figure 3, where the smallest value of the band gap between occupied and unoccupied states is considered. For devices this is convenient as the thickness can be represented on the x-axis.

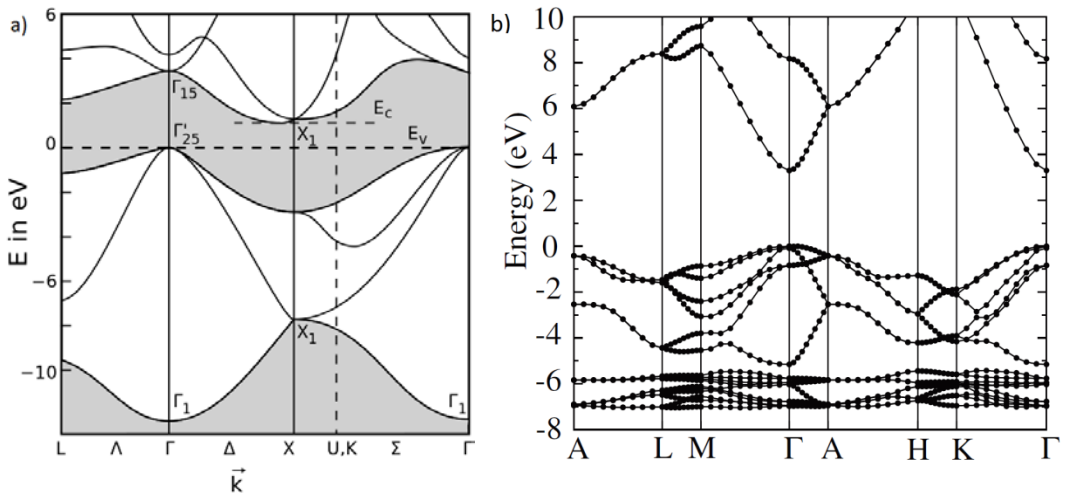

Figure 2 – The $E(k)$ diagrams for silicon and zinc oxide showing direct and indirect band gap respectively. For silicon forbidden energies are indicated by the shaded regions, the band gap E_g is given by $E_C - E_V$ as indicated. For zinc oxide the direct band gap is at the Γ-point with E_V set to zero. The figures are reproduced from [14] and [15].

At 0 K the electrons occupy the lowest available energy levels, leaving all higher energy levels unoccupied. Then the highest occupied energy level constitutes a boundary which is known as the Fermi energy. The Fermi energy is not to be confused with the Fermi level which is to be described in the next section. The location of the Fermi energy relative to the band edges determines whether the material is characterized as a metal, a semiconductor or an insulator. As can be seen in Figure 3 metals have the Fermi energy within a band. This implies that even the smallest change in energy will allow an electron to move into other available energy levels. Hence the electron is mobile and can easily contribute to an electrical current. For semiconductors and insulators the Fermi energy is located at the top of a band, this band is called the valence band. The next band across the band gap is called the conduction band and is empty in the 0 K groundstate. The magnitude of the band gap is used to separate semiconductors from insulators. Materials with low band gaps are called semiconductors, while materials with band gaps higher than $\sim 5\ eV$ are called insulators, the boundary being somewhat gradual and different depending on whom is asked and in what context.

When using the simplified band diagram of Figure 3, some properties of the $E(\boldsymbol{k})$ relationship must be kept in mind as they describe important materials properties. The first is the notion of whether the material has a direct or indirect band gap. A direct band gap has the valence and conduction band extremes located at the same value of $\boldsymbol{k}$, while indirect band gaps have a separation between these. As can be seen in Figure 2 silicon has an indirect band gap, while zinc oxide has a direct one. This affects the mechanism of interaction of electrons between the valence band and the conduction band. In a direct band gap material the emission of a photon can take place directly by recombination of an excited electron from the conduction- to the valence band. In indirect band gap materials a change in momentum is also needed. This momentum change cannot be provided by the photon as it is a mass less particle. Instead it has to come from interaction with a lattice vibration, called a phonon. This extra demand implies that the direct transitions are more likely and thus the lifetime of excited electrons are often higher in materials with indirect band gap. Also the curvature of the bands carries information of physical properties. The periodic potential influence the charge carriers in a way that is

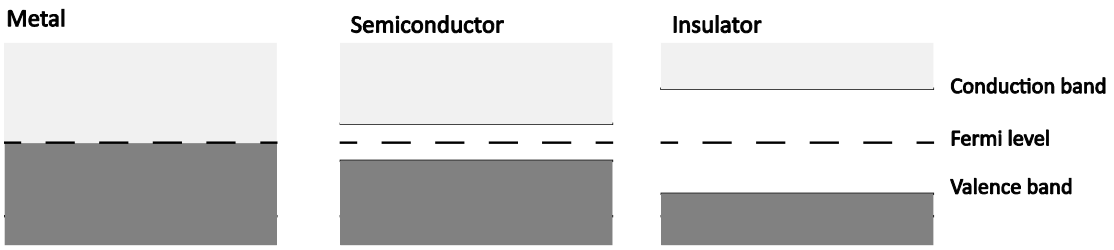

Figure 3 –Simplified band diagrams for metals, semiconductors and insulators.

commonly incorporated as an effective mass, i.e. a pre-factor to the electron rest mass used in calculations. The density of states (DOS) in the bands is also affected, and for calculations parabolic functions are used to approximate the band curvature.

2.3.2 CHARGE CARRIERS

A pure, un-doped semiconductor is called an intrinsic semiconductor. An electrical current cannot take place unless an electron is excited from the valence band into the conduction band. Energy equal to, or larger than, the band gap is needed for such an excitation and the resulting electron in the conduction band is free to move in the available states. In addition, the electron leaves behind an unoccupied state in the valence band. This state is called a hole, and when another valence electron moves into the hole, the hole itself effectively moves in the other direction as a positive charge carrier contributing to the current. At non-zero temperatures the distribution of thermal energies of the electrons in the system provides a rate at which electrons are excited into the conduction band. At thermal equilibrium this rate is balanced by a recombination rate, which is the rate at which electrons fall back and recombine with holes in the valence band. This gives a steady state concentration of electron-hole pairs (EHP) with electron concentration in the conduction band n equal to the hole concentration in the valence band p so that $n = p = n_i$ where n_i is the intrinsic carrier concentration.

Calculating the concentration of charge carriers in a semiconductor can be done by evaluating an integral of the product of density of states and the energy distribution of the charge carriers. For electrons this can be written:

$$n = \int_{E_C}^{\infty} N(E) f(E) dE \tag{2.2}$$

And for holes:

$$p = \int_{-\infty}^{E_V} N(E)\big(1 - f(E)\big) dE \tag{2.3}$$

where $N(E)$is the density of states as function of energy, and $f(E)$ is the Fermi-Dirac distribution function giving the probability of a state at energy E being occupied at any given temperature:

$$f(E) = \frac{1}{1 + e^{\frac{E-E_F}{kT}}} \tag{2.4}$$

The thermal energy is the product of the temperature T and Boltzmann's constant k. E_F is the Fermi level which is equivalent to the chemical potential for the electrons. If an electronic state is available at the Fermi level it is characterized with a probability of occupation equal to one half, but the existence of such a state is not necessary for the definition of the Fermi level. For an intrinsic semiconductor the Fermi level is close to the middle of the band gap, with the deviation coming only from difference in density of states in the conduction and valence band. For doped materials the Fermi level is shifted towards the appropriate band. The Fermi-Dirac function takes the shape of a step function at zero temperature, and smears out at increasing temperatures.

If the Fermi level position is sufficiently far from the energy level that is considered the Fermi-Dirac distribution can be simplified to a Boltzmann expression. Further, for relatively low doping levels, it is appropriate to evaluate the charge carrier concentration at the band edges as the distribution tails of rapidly above this level. Then the integrals simplifies to:

$$n = N_C f(E_C) = N_C e^{-\frac{E_C - E_F}{kT}} \tag{2.5}$$

$$p = N_V\big(1 - f(E_V)\big) = N_V e^{-\frac{E_F - E_V}{kT}} \tag{2.6}$$

Here, N_C and N_V are the effective density of states for the conduction and valence band edges, respectively. The density of states at the conduction band edge is given by:

$$N_C = 2\left(\frac{2\pi m_n^* \, kT}{h^2}\right)^{\frac{3}{2}}, \tag{2.7}$$

and for the valence band, only the m_n^* factor is exchanged for m_p^*. These are effective masses for electrons and holes respectively, h is the Planck constant.

For doped materials the concentration of electrons and holes are no longer equal, this is because the dopants are compensated by either an electron or a hole. Doping of silicon will be considered to elaborate on this. Phosphorus has one more valence electron than silicon, and thus has a left-over electron after the bonds to the nearby silicon atoms are satisfied. This electron is weakly bonded to the phosphorus atom and will be delocalized in the material by thermal energy even at low temperatures. Donation of the electron leaves a stationary positive ion, and phosphorous is known as a donor dopant. In the band structure this corresponds to emptying an initially filled electron state close to the conduction band. Using the notation of defects the mechanism can be written $P_{Si}^{x} = P_{Si}^{\bullet} + e^{/}$. Boron on the other hand has one valence electron less than silicon, and to satisfy the bonds to its neighbors it must accept an electron from the surroundings, making it an acceptor dopant. The captured electrons give a mobile deficiency of valence electrons i.e. holes in the valence band denoted $h^{\bullet}$by the mechanism $B_{Si}^{x} = B_{Si}^{/} + h^{\bullet}$. If both donors and acceptors are present they compensate each other, and the total charge neutrality condition becomes $p + N_D = n + N_A$. In a material with larger concentration of donors, electrons are the dominating charge carrier and the material is called n-type,

while materials dominated by acceptors are called p-type. The conductivity of semiconductors is given by:

$$\sigma = q(n\mu_n + p\mu_p) \tag{2.8}$$

where q is the elementary charge and $\mu_{n,p}$ is the mobility for electrons and holes. The mobility is a material property given by the drift velocity achieved in an electric field.

From this discussion it can be understood that the conductivity in an intrinsic semiconductor is strongly temperature dependent. In doped materials, the doping concentration controls conductivity through the electronic compensation of the dopants in a wide temperature range. Low temperatures are needed to freeze out the typical dopants, meaning that they are not ionized and contribute charge carriers. With normal doping concentrations and band gaps above $\sim 1\ eV$, high temperatures are needed before intrinsic thermal excitation becomes dominating.

2.3.3 Amorphous semiconductors

The lack of long range order in an amorphous solid comes from fluctuations in the length and angle of the interatomic bonds. These variations smear out the band energies resulting in less clearly defined band edges, seen as so called Urbach tails extending into the band gap. The lack of long range order also removes the symmetry differences seen in different crystallographic directions in crystalline solids. The notion of direct and indirect materials thus loses meaning, and all amorphous semiconductors are found to behave similar to that of direct band gaps. Yet another result of the lack of periodicity is what is called dangling bonds. These are unfinished bonds between atoms, meaning valence electrons that do not contribute to a bond, or orbitals lacking in electrons. Dangling bonds may thus be associated with a charge and can, for instance, contribute to deep levels in the band gap. [16]

2.3.4 Deep levels

The present subsection will address the properties of deep levels leading to equations of interest with respect to Deep Level Transient Spectroscopy (DLTS), and is based on Blood and Orton's [17] work. DLTS is the characterization method used in this thesis, described in chapter 5.4.

As seen above, the intentional doping with specific substitutional defects introduce states close to the band edges. Other defects may introduce states deeper into the band gap. With energy separation between the defect state and the band edge larger than $\sim 0.05\ eV$ a defect state is often characterized as deep. For deep states the doping efficiency is often reduced and instead these states may act as traps or recombination centers. Trapping occurs when a state captures and holds a charge carrier and thus inhibits its contribution to conduction, while recombination centers capture both electrons and holes effectively assisting their recombination. Even for small concentrations this behavior can severely limit the lifetime of excited charge carriers which is a problem in many applications and especially photovoltaics.

Along with the location in the band gap the deep levels are characterized by a capture cross section. The energy level and capture cross section are known collectively as the trap signature. Rates of capture and emission from the deep levels are related to the trap signature, and determine their

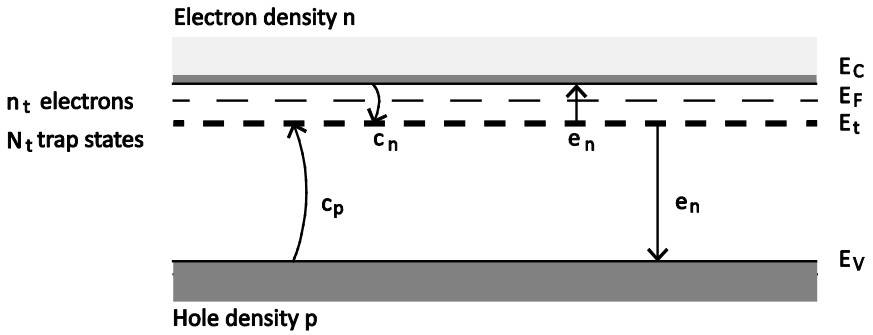

Figure 4 – A trap level and its interaction mechanisms with the conduction- and valence band is shown. From left to right: hole capture, electron capture, electron emission and hole emission.

efficiency as traps and recombination centers. The derivation of expressions for deep levels thus starts with considerations about the different rates and their equilibrium relations.

CARRIER INTERACTION RATE WITH TRAPS

Figure 4 shows the different capture and emission processes for traps with energy level E_t. The concentration of a trap is labeled N_t and the electron occupancy of the trap is labeled n_t. c_n is the capture rate of electrons from the conduction band, and c_p of holes from the valence band. Similarly, e_n and e_p are emission rates from the trap.

Electron capture and hole emission depend on the concentration of unoccupied traps and act to increase the occupancy, while electron emission and hole capture depend on the occupied traps to decrease the occupancy. This is summarized in equation (2.9), where a and b are just collective terms for increasing and decreasing occupancy, respectively.

$$\frac{dn_t}{dt} = \big(c_n + e_p\big)(N_t - n_t) - \big(e_n + c_p\big)n_t = a(N_t - n_t) - b\, n_t \tag{2.9}$$

At thermal equilibrium the change in occupancy is zero, and there can be no build-up of charge carriers on the trap. This leads to a detailed balance:

$$\begin{aligned} e_n n_t &= c_n(N_t - n_t) \\ e_p\,(N_t - n_t) &= c_p n_t \end{aligned} \tag{2.10}$$

By rearrangement the equilibrium occupancy $\hat{n}_t$ is expressed as

$$\frac{\hat{n}_t}{N_t} = \frac{c_n}{c_n + e_n} = \frac{e_p}{e_p + c_p} \tag{2.11}$$

This occupancy can also be expressed by the Fermi-Dirac distribution:

$$\frac{\hat{n}_t}{N_t} = \left(1 + \frac{g_0}{g_1} e^{\frac{E_t - E_F}{kT}}\right)^{-1} \tag{2.12}$$

Here, g_0 and g_1 are the degeneracy of the unoccupied state and the state occupied by one electron, their ratio is close to unity and omitted in the following derivation. By combining these expressions a ratio between the emission and capture rate for the carriers is obtained:

$$\frac{e_n}{c_n} = e^{\frac{E_t - E_F}{kT}} \tag{2.13}$$

$$\frac{e_p}{c_p} = e^{\frac{E_F - E_t}{kT}} \tag{2.14}$$

For the special case of $E_t = E_F$ the ratio between emission and capture rates is close to unity. A higher Fermi level position implies that the electron gain mechanisms dominate and the trap is occupied, while the opposite is true for a Fermi level lower than the trap level. This change in the rate ratios is related to the probability of occupation of states described by the Fermi-Dirac distribution given in equation (2.4).

CAPTURE RATE

After the use of the capture and emission rates in the above derivation of occupancies and ratios, it is time to define properly the meaning of the rates. To do so capture of electrons is considered, while the derivation of an expression for hole capture can be done in a similar manner. Assume a change in trap occupancy Δn_t comes solely from electron capture in a short time Δt. This gives

$$\Delta n_t = \sigma_n n \langle v_n \rangle (N_t - n_t) \Delta t \tag{2.15}$$

where σ_n is the capture cross section for electrons of the trap. The concentration of free electrons n multiplied with the root mean square of the thermal velocity $\langle v_n \rangle$ yields the flux of electrons. $(N_t - n_t)$ is as before the concentration of unoccupied traps, i.e. those available for trapping. From this the capture rate per unoccupied trap state is defined

$$c_n = \frac{\frac{\Delta n_t}{\Delta t}}{N_t - n_t} = \sigma_n \langle v_n \rangle n \tag{2.16}$$

EMISSION RATE

As seen above the capture rate depends on the doping of the material through the concentration of free charge carriers. The emission rate on the other hand is an intrinsic property of the trap. Continuing to use electrons as the example an expression for the emission rate can be found by inserting equation (2.16) into (2.13), using equation (2.5) for n:

$$e_n(T) = \sigma_n \langle v_n \rangle N_C e^{-\frac{E_C - E_t}{kT}} \tag{2.17}$$

This expression has a temperature dependency given by several of the factors:

$$\langle v_n \rangle = \left(\frac{3kT}{m^*}\right)^{\frac{1}{2}}$$

$$N_C = 2M_C\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}}$$

here M_C is the number of conduction band minima, and the other entities have their usual meaning. The capture cross section may also have a temperature dependence with activation energy ΔE_σ and a value $\sigma_\infty$when extrapolated to infinite temperature.

$$\sigma_n(T) = \sigma_\infty e^{-\frac{\Delta E_\sigma}{kT}}$$

Inserting these expressions into equation (2.17) gives the emission rate, or more correctly emission rate per trapped electron:

$$e_n(T) = \gamma T^2 \sigma_{na} e^{-\frac{E_{na}}{kT}} \quad \textbf{(2.18)}$$

Here the physical constants are collected in $\gamma = 2\sqrt{3}\, M_C (2\pi)^{\frac{3}{2}} k^2 m^* h^{-3}$. The extrapolated infinity-temperature capture cross section is modified by the degeneracy ratio to give an apparent capture cross section $\sigma_{na} = \frac{g_0}{g_1}\sigma_\infty$. E_{na} is the activation energy, $E_{na} = (E_C - E_t) + \Delta E_\sigma$, which deviates from the trap energy level by ΔE_σ. Determination of these values further assumes that $(E_C - E_t)$ does not change with temperature.

TRAP SIGNATURE

Equation (2.18) is an important tool in the analysis of traps. A so called trap signature plot can be made on semi-logarithmic axes by plotting $\frac{e_n}{T^2}$ versus T^{-1}. This produces a straight line where σ_{na} can be deduced from the intercept with the y axis and $E_{na}$from the slope. Experimental data fit this expression over orders of magnitude of e_n for most traps. However, σ_{na} and E_{na} do not exactly represent the desired values which are the real capture cross section σ_n and the separation of the trap energy level and the band edge $(E_C - E_t)$. Looking at the thermodynamics might help the understanding of the differences between these values. The energy required to remove an electron from a trap into the conduction band is an ionization energy, that is the same as a chemical potential or change in Gibbs free energy $\Delta G = E_C - E_t$.Changes in Gibbs free energy can be separated into enthalpy and entropy parts by the thermodynamic identity $\Delta G = \Delta H - T\Delta S$. Inserting this into equation (2.17) a new expression is obtained:

$$e_n(T) = \sigma_n \langle v_n \rangle N_C e^{-\frac{\Delta G}{kT}}$$

$$e_n(T) = e^{\frac{\Delta S}{k}} \sigma_n \langle v_n \rangle N_C e^{-\frac{\Delta H}{kT}} \quad \textbf{(2.19)}$$

Comparing equation (2.18) and (2.19), the activation energy (E_{na}) is actually the enthalpy of formation of the ionization, while the apparent capture cross section includes the entropy term $\sigma_{na} = e^{\frac{\Delta S}{k}}\sigma_n$.

Depending on their origin, deep levels can be either occupied or unoccupied when neutral. Analogous to the shallow dopant levels, the deep levels then behave either donor-like or acceptor-like, respectively. Regardless of which type, the trap levels may interact with both the valence and conduction band. In DLTS, as will be discussed in section 5.4, it is interaction with the majority carrier band that is studied, and thus the deep levels' properties as majority carrier traps that is determined.

2.4 PN-JUNCTION

Good junctions between n-type and p-type materials can be made for many materials systems, either by production of layered material structures or by diffusion or implantation of dopants into a material. A perfect metallurgical junction is assumed in the following treatment, with uniform doping concentration in each material. This gives a sharp step in concentration at the junction.

2.4.1 EQUILIBRIUM PROPERTIES

The sharp step in mobile charge carriers gives diffusion into the opposite material. This leaves ionized dopant atoms in a volume adjacent to the junction. Equilibrium is reached when the ionized dopants produce an electric field $\mathcal{E}$ that is strong enough to provide a drift current that exactly balances the diffusion current. Two assumptions comprise the depletion approximation easing the mathematical treatment of this situation; *(i)* the depletion of charge carriers due to diffusion and recombination is complete in a region of width W around the metallurgical junction. Space charge in this depletion region is given solely by the ionized donors N_d on the n-side and acceptors N_a on the p-side. *(ii)* Outside the depletion region there is no space charge and thus no electric field. Charge neutrality considerations demand that the total amount of charge Q from the dopant ions must be equal on the n- and p-side. Thus the extent of the depletion region on either side depends on the doping concentration through:

$$|Q| = qAN_d x_n = qAN_a x_p \tag{2.20}$$

Where q is the elementary charge, A is the area of the junction, and $x_{n,p}$ are the depths of the depletion region from the junction in the n- and p-type materials. The electric field has a negative value as it goes from n-type to p-type, with the highest numerical value found at the junction. Solving the Poisson equation $\Delta^2 V = -\Delta\mathcal{E} = \rho/\varepsilon$, with ρ as the charge density and ε the permittivity, and using the depletion approximation, the maximum field can be found:

$$\mathcal{E}_0 = -\frac{q}{\varepsilon} N_d x_n = -\frac{q}{\varepsilon} N_a x_p \tag{2.21}$$

Further, the field is related to the spatial variation of the potential as:

$$\mathcal{E}(x) = -\frac{dV(x)}{dx} \tag{2.22}$$

Using the depletion approximation again it follows that the potential outside the depletion region is constant at V_n and V_p on the n- and p-side. The difference in the potentials on each side of the junction, i.e. $V_0 = V_n - V_p$, is known as the built-in voltage or contact potential. Related to the difference in

potential, the band structure is also shifted as the junction is formed. This displacement of the bands can also be understood by considering the Fermi level. The Fermi level must be constant throughout the material in equilibrium and as a result the bands must bend to connect in the depletion region. The band structure over the junction is shown for zero bias in the center pane of Figure 5. Rearranging equation (2.22) one can solve for the contact potential:

$$-V_0 = \int_{-x_p}^{x_n} \mathcal{E}(x)\, dx = \frac{1}{2}\mathcal{E}_0 W \tag{2.23}$$

$$V_0 = \frac{1}{2}\,\frac{q}{\varepsilon} N_d x_n\, W \tag{2.24}$$

Using $W = x_n + x_p$ and simplifying equation (2.20) to $N_d x_n = N_a x_p$ gives:

$$x_n = \frac{W N_a}{N_d + N_a} \tag{2.25}$$

So:

$$V_0 = \frac{1}{2}\frac{q}{\epsilon}\left(\frac{N_d N_a}{N_d + N_a}\right) W^2 \tag{2.26}$$

Rearranging with respect to the depletion width one obtains:

$$W = \left(\frac{2\varepsilon}{q}\left(\frac{1}{N_d} + \frac{1}{N_a}\right) V_0\right)^{\frac{1}{2}} \tag{2.27}$$

which is widely used.

2.4.2 Applying a bias voltage

Applying an electric field, or a bias voltage, to the junction disrupts the equilibrium described in the previous section. The built-in voltage determined the depletion width in equilibrium, but W is now determined by the total junction voltage, $V_j = V_0 - V$ where V is the externally applied bias. The Fermi level is only defined under equilibrium conditions; however, it is instructive to define so called quasi Fermi levels which are separated by energy qV.

Changes in the band structure follow from the Fermi level splitting, as illustrated in Figure 5 for two different biasing situations. Also, the balance between the drift and diffusion current is shifted. A forward bias is defined as the application of a positive voltage on the p-type relative to the n-type side of the junction, and positive values for V are used. This decreases the potential difference and thus the barrier in the energy band diagram. It can be shown that diffusion across the junction increases exponentially with the applied voltage as the electric field is lowered along with the barrier. Biasing in the other direction is called reverse bias. This expands the depletion width and increases the potential difference, i.e. the barrier, and the electric field. The effect is that the diffusion current is quenched, and the drift current will be dominating. Although an increasing drift current could be suspected with increasing reverse bias, this is not the case as it is the low concentration of minority carriers that limits

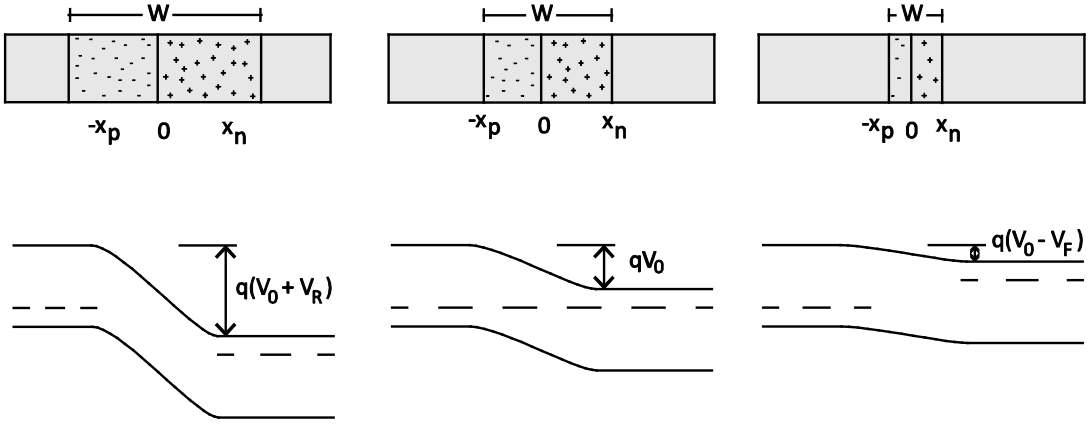

Figure 5 – Reverse bias (left) increase the depletion width and the energy barrier compared to the zero-bias situation (middle). Forward biasing reduces depletion width and current can flow more freely across a lowered barrier.

this current and not the speed with which they are transported across the junction. Therefore, the reverse saturation current is found to depend on the rate at which minority carriers arrive at the depletion region edges. This again depends on the carrier concentrations in the material and diffusion properties and does not depend on the magnitude of the reverse bias. With the reverse saturation current I_0 given by the drift current from generation of minority charge carriers, the total current as a function of the applied voltage is expressed by the ideal diode equation:

$$I(V) = I_0\left(e^{\frac{qV}{kT}} - 1\right) \tag{2.28}$$

This means that the junction is asymmetrical in terms of conductance, showing rectifying behavior with regard to applied voltage. Such a device is known as a diode in electronics.

Depending on material and fabrication processes, a real diode might have properties that deviate from the ideal model in several ways. The model assumes that there is no generation or recombination in the depletion region. Recombination becomes significant when the depletion region is wide due to low doping or low forward bias. Also defect levels in the band gap can facilitate recombination. This can be accounted for by including an ideality factor n in the ideal diode equation:

$$I(V) = I_0\left(e^{\frac{qV}{nkT}} - 1\right) \tag{2.29}$$

For reverse bias, recombination is not substantial in the depletion region as the large electric field is likely to sweep any charge carriers across the depletion region before they are able to recombine. Generation might however take place and contribute to large deviations from the ideal reverse saturation current. Ohmic loss in the neutral regions is also a known deviation, especially relevant at high forward biases. A sketch of the different discrepancies is shown in Figure 6 on a semi-logarithmic plot along with the ideal model.

2.4.3 Depletion capacitance

Capacitance is the ability of a device to store an electric charge Q and it is defined as $C = |Q/V|$ for capacitors with linear capacitance-voltage relationship. The depletion region capacitance, however,

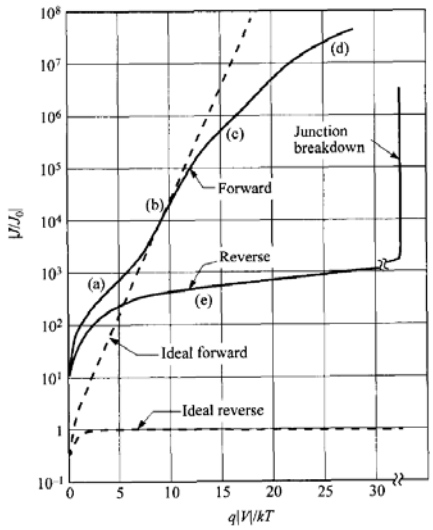

Figure 6 – Forward and reverse characteristics for ideal and non-ideal diode on a semi-logarithmic plot from Sze [18]. At low forward bias the real diode is dominated by generation and recombination (a). Ideal behavior from diffusion current is seen in (b), while high injection and series resistance dominate in (c) and (d). The high reverse current is attributed to surface effects and generation and recombination.

varies non-linearly with the voltage. This arises from the non-linear relationship between the voltage and the charge. The charge is given in equation (2.20), and inserting equation (2.25) results in:

$$|Q| = qA\left(\frac{N_d N_a}{N_d + N_a}\right)W \tag{2.30}$$

In the expression for the depletion width it is necessary to account for the external voltage, as described in the previous section so that V_0 is replaced by V_j in equation (2.27). Then, the non-linearity is clear, and a more general definition of capacitance, $C \equiv |dQ/dV|$, must be used. Solving this yields an expression equivalent to the solution for parallel plate capacitors:

$$C = A\left(\frac{q\varepsilon}{2V_j}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)^{-1}\right)^{\frac{1}{2}} = \frac{\varepsilon A}{W} \tag{2.31}$$

2.4.4 Asymmetrical junctions

An asymmetrical junction is a junction where one side is doped more heavily than the other. A simple notation for this is to add a superscript + on the most heavily doped side, e.g p^+n denotes a diode with more heavily doping on the p-side. Rearranging equation (2.20) yields $\frac{x_p}{x_n} = \frac{N_d}{N_a}$, showing that the extent of the depletion region will be dominated by the weakly doped side. This is reflected in the capacitance expression of equation (2.31) where the lower doping dominates. The capacitance becomes:

$$C = A\sqrt{\frac{\varepsilon q}{2V_j}N_{a,d}} \tag{2.32}$$

where the subscript refers to the low-doped side of the junction.

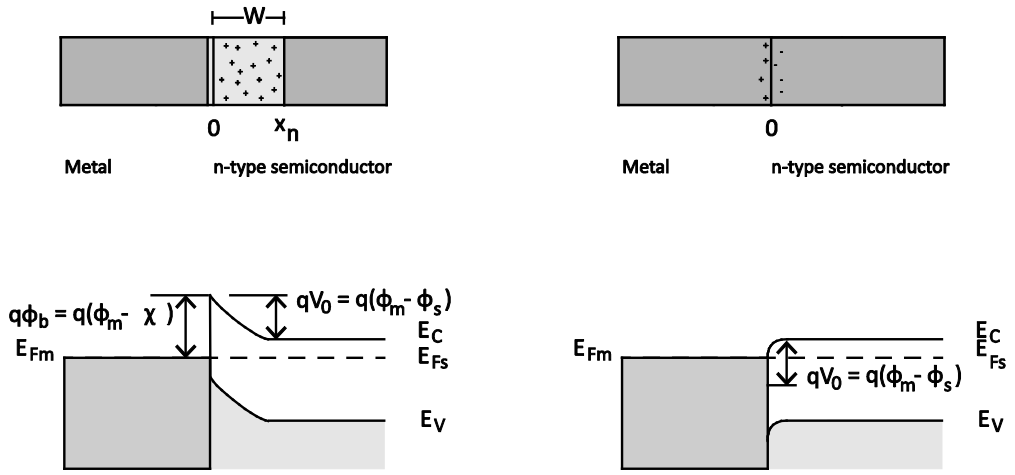

Figure 7 – Schottky and Ohmic contact between metal and semiconductor. Ideally, unless Fermi pinning occurs, the type of contact is determined by the Schottky-Mott rule.

2.5 SCHOTTKY- AND HETEROJUNCTIONS

The pn-junctions discussed above are assumed to be made of the same material with different doping in the different regions and are called homojunctions. However, rectifying junctions occur also between different materials. Metal-semiconductor junctions will be considered briefly here, as well as junctions between semiconductors with different band gaps, also known as heterojunctions.

2.5.1 METAL-SEMICONDUCTOR JUNCTIONS

When a metal and a semiconductor are brought into contact the Fermi levels has to align as in the case for the pn-junction. For the following discussion it is convenient to introduce another energy level in the band diagram; that is the vacuum level. The energy $q\phi$ separates the vacuum level from the Fermi level, and ϕ is known as the work function. The separation from the semiconductors conduction band to the vacuum level is $q\chi$ where χ is the electron affinity. The alignment of the Fermi levels can cause a continuous bending of the vacuum level into the semiconductor. According to the Schottky-Mott model this bending is equal to the bending of the valence and conduction band. Thus, discontinuities in the available states occur at the interface, resulting in barriers for the charge carriers. If the barrier is large, the band bending causes depletion of the majority carriers in the semiconductor and the junction will be rectifying. The behavior will then be similar to an asymmetrical pn-junction since the mobile charges of the metal can accumulate in a negligible depth at the interface. If there is no depletion following from the alignment of the Fermi levels the contact is Ohmic. Ohmic contacts are essential in connecting devices to external circuits, and are, indeed, important for the work in this thesis. Ohmic behavior can also be achieved with metal on a highly doped semiconductor, then the depletion region is narrow and electrons may tunnel through the barrier. In Figure 7 the band diagrams for Schottky- and ohmic contacts between a metal and an n-type semiconductor are shown.

The discontinuity in the Schottky contact gives a barrier height $\phi_{bn} = \phi - \chi$ for electrons, as seen in Figure 7. The barrier height for Schottky diodes to p-type semiconductors is given by $\phi_{bp} = \chi - \phi + E_g$. From this it can be seen that the sum of the barrier height should equal the band gap if two Schottky contacts are made on respectively n-type and p-type semiconductor with the same metal.

However, deviations are frequently encountered in real systems, attributed to non-ideal interfaces with electron states within the band gap, as described by Bardeen [19]. This effect is called Fermi level pinning as band bending occurs from alignment, or pinning, to defect levels and thus diminishing the importance of the metal work function.

Applying a voltage across the Schottky contact shifts the band structure and the depletion region similar to that of a pn-junction and the same diode equation can be used to describe the current. The difference is in the origin of the reverse saturation current I_0. The Schottky contact is a majority carrier device, so with n-type semiconductor there is no hole conduction across the junction. Instead the reverse saturation current comes from thermal excitation of electrons across the barrier. This is described by the thermionic emission theory:

$$I_0 = A^* A T^2 e^{-\frac{\phi_b}{kT}} \tag{2.33}$$

The exponential term gives the fraction of electrons with energy higher than the barrier height at thermal energy kT. A is the area of the diode. The Richardson constant is given by

$$A^* = \frac{4\pi q m_{n,p}^* k^2}{h^3} = \left(120 \frac{A}{cm^2 K^2}\right) \frac{m_{n,p}^*}{m_0} \tag{2.34}$$

and is a constant determined by the effective mass of the charge carriers in the material, m_0 is the electron rest mass.

In real devices, the reverse current from thermionic emission theory may be accompanied by other conduction mechanisms. If the barrier is sufficiently narrow, tunneling might occur through the barrier, this is known as field emission. The combination of these two is thermionic field emission, which is tunneling through the barrier, but at an elevated energy where the barrier is narrower than at the 'base'.

2.5.2 HETEROJUNCTIONS

As with Schottky contacts discontinuities in the band structure is expected in heterojunctions. This is a result of the differences in electron affinity and band gap. Aligning the Fermi levels, and keeping a continuous vacuum level, the difference in band gap ΔE_g must be divided between the conduction band ΔE_C and the valence band ΔE_V. Analogous to the Schottky-Mott model for metal-semiconductor junctions this discontinuity is described with the Anderson affinity rule. This states that the conduction band offset is given by the difference in electron affinities, $\Delta E_C = q(\chi_2 - \chi_1)$, and the rest of the band gap difference is in the valence band, $\Delta E_V = \Delta E_g - \Delta E_C$. Three different classes of heterojunctions are possible, as illustrated in Figure 8. An important consequence of this is that, contrary to homojunctions, heterojunctions may have very different properties for electrons and holes. This is because the discontinuities act differently on the different bands. [18] It is also possible to achieve barriers and rectification in so called isotype heterojunctions; these are junctions of two materials with the same doping (n- or p-type).

Utilizing different materials allows tailoring of the band structure to specific needs; this is called band gap engineering. In some material systems careful alloying enables tuning of the band gap in a wide

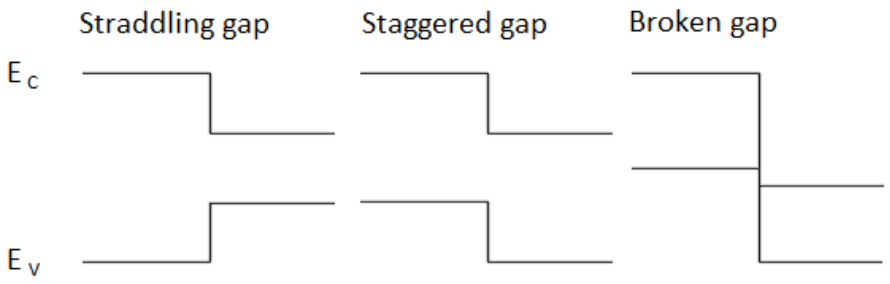

Figure 8 – Three variations of heterojunction band alignment.

range which is sought after in many devices, including LEDs and laser diodes. A drawback with heterostructures is as for Schottky contacts, the challenge of high quality interfaces. Fermi level pinning can give band offsets deviating significantly from the theoretical model depending on the interface quality and material properties.

2.6 SOLAR CELLS

Most solar cell technologies are based on semiconducting materials, although other ideas exist such as organic cells based on polymers. A variety of different semiconductor materials and production techniques are used, and it is common to make a separation between thin-film and bulk technologies. Thin-film cells consist of thin active layers, normally deposited onto a cheap substrate, and are attractive due to low material consumption. The market, however, is dominated by bulk silicon technologies, shared between multi- and mono-crystalline silicon. Regardless of technology there are three demands that must be fulfilled in order to produce electricity from sunlight. (i) Generation; the material must absorb the incoming photons by exciting electrons to a higher energy state, in semiconductors the excitation is from the valence to the conduction band and an electron-hole pair results. (ii)Separation; a means of separating the electrons and holes must exist in order to avoid recombination. The pn-junction provides the driving force for separation. (iii) Extraction; an external circuit must be able to utilize the increased energy from the excited electrons by drawing a current.

For a semiconductor the pn-junction properties make the basis for the active part of the solar cell. In the next subsection the construction of silicon based solar cells will be reviewed briefly. A summary of mode of operation and figures of merit follows, and then some design alternatives relevant to this work are reviewed in the last subsections. This is primarily based on the work by Nelson [16].

2.6.1 PRODUCTION OF A SILICON SOLAR CELL

The production of a standard silicon based solar cell starts with reduction of silicon from the silicon dioxide mineral quartz. Purification steps follows, and *solar grade* Si (SOG-Si) with impurity concentrations on the order of parts per million (ppm) are obtained. This purification is usually done with the Siemens process, while development of new, less energy demanding, methods is a primary concern [20, 21]. The next step is to produce high quality wafers. Price versus performance considerations must then be made in the choice between multi- and mono-crystalline silicon. Multi-

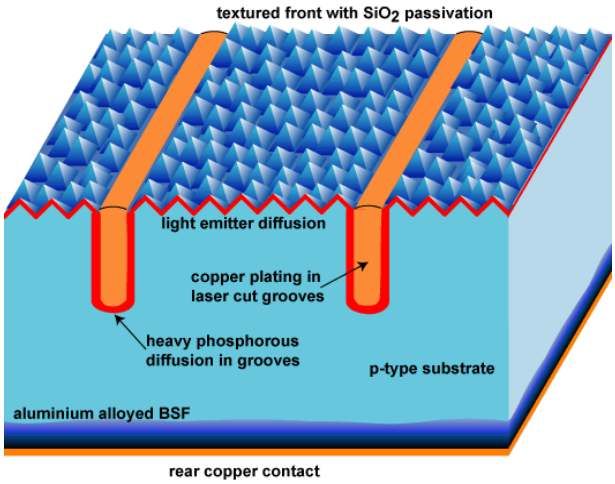

Figure 9 – Cross section of a solar cell with surface texturing and buried front side contacts. The figure is reproduced from [23].

crystalline silicon is relatively cheap to produce, but the grain boundaries have high defect densities and thus facilitate recombination which reduces the final efficiency of the cell. Several production methods are used, including casting and ribbon growth, with the common focus to produce large grained materials. The grains should be at least on the same scale as the wafer thickness in order to minimize the challenges with recombination. Mono-crystalline silicon is on the other hand free of grain boundaries giving a high efficiency with the drawback of advanced and expensive production methods, where the Czochralski process is the most widely used [22]. Starting from a crucible of molten silicon a crystalline seed is dipped and then pulled up. By controlling the pulling speed and rotation a perfect crystal grows at the solid-liquid interface, and cylindrical ingots with diameter of 30 cm and lengths of 2 m are industrially available. A base doping, typically p-type with boron, is added to the melt before solidification. The ingots or cast are then sawn to wafers of typical thickness in the 0.2 to 0.5 mm range.

The wafers comprise the base of the cell and the next step is to make a shallow n-type layer called the emitter on the front surface. This can be done in by diffusion of phosphorous from a gas phase or by ion-implantation. Ion-implantation is expensive and thus not widely used in PV, but gives excellent control over the dose and depth, and an abrupt junction. The diffusion method gives a graded junction, as the diffusion profile is specific to the material system, but is cheaper to perform. Either way a doping concentration in the order of $10^{19}\ cm^{-3}$ is required to ensure high conductivity to the external circuit. Absorption, particularly of the high energy photons from the blue and Ultra Violet (UV) part of the spectrum, is predominant close to the surface. A shallow junction, close to the front surface, is thus necessary since excited electron-hole pairs must be close to the depletion region in order to be separated. Otherwise, recombination will occur and the excitation energy is wasted.

A cross sectional illustration of a solar cell is shown in Figure 9. When the pn-junction is produced the remaining steps are to improve absorption and make contacts for the external circuit. Texturing of the front side and deposition of antireflective coatings make sure that as much as possible of the incoming light enters the material. Etches that are selective in terms of crystalline directions are conveniently used to shape pyramids on the surface, this way light that is reflected off the surface will

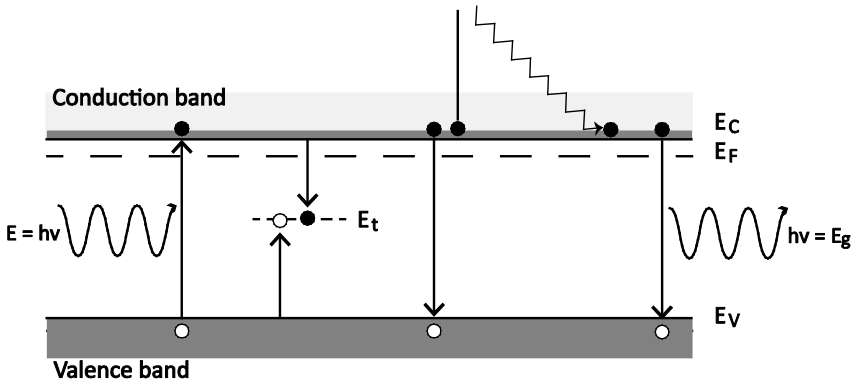

Figure 10 – Generation and recombination processes. From left: (i) Generation of an electron-hole pair by an incident photon of energy $h\nu$. (ii) Trap assited recombination, also known as Shockley-Read-Hall (SRH) recombination. (iii) Auger recombination involves two electrons colliding in the conduction band, one recombine to the valence band while the other is excited to a higher energy followed by thermalization. (iv) direct radiative recombination gives emission of a photon with energy corresponding to the band gap energy.

be incident on another pyramid, increasing the probability of absorption. The antireflective coatings used are materials with well-tailored thickness and refractive index. A refractive index between that of air and silicon is used to reduce the reflection; silicon nitride (Si_3N_4) is suitable for this purpose. The thickness of this coating is made to correspond to a quarter of the wavelength of some wavelength in the spectrum. For this particular wavelength reflection from the surface and the interface to the silicon will have destructive interference thus quenching the reflection. Other wavelengths will still be reflected, so an idealization must be made with respect to the material properties and the solar spectrum. Designing the front side contacts is a compromise between the ability to effectively collect as many as possible of the generated electrons and shading as little as possible of the area of the active material. In this example buried contacts is shown, covering a minimum of the surface area.

2.6.2 Operation mechanism and figures of merit

Batteries are generally viewed as voltage generators, delivering a fairly constant voltage for a large span of external loads. Solar cells on the other hand are more correctly viewed as current generators where the current output is proportional to the illumination rather than to the load. When a solar cell is illuminated, excess charge carriers are generated due to optical excitation across the band gap. The generation process is illustrated in Figure 10, along with three different recombination mechanisms. If the generated electron-hole pairs reach the depletion region before they have time to recombine, the contact potential of the pn-junction will separate them and a contribution to the drift current results. Depending on the external circuit two extremes can be identified. At open circuit conditions, that is with no external circuit connected, there can be no net current. A potential called the open circuit voltage V_{OC} then builds up across the cell. Short circuiting the cell is the other extreme, then the voltage is quenched and the photo-generated current flows freely. This current is called the short-circuit current I_{SC}, and can be expressed:

$$I_{SC} = qA \int b_s(E) QE(E) dE \tag{2.35}$$

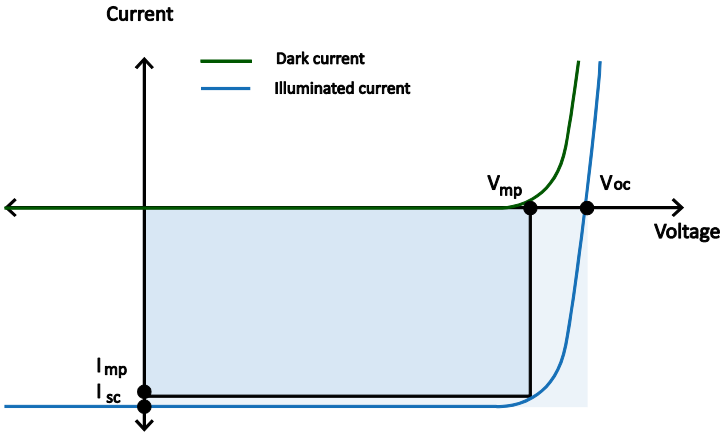

Figure 11 – The darker shading illustrates the maximum power output, and its ratio to the lighter shaded region is the fill factor FF.

Here q is the elemental charge, A is the area of the cell, $b_s(E)$ is the flux density of photons with energy E and $QE(E)$ is the quantum efficiency. The latter is the probability for an incident photon to contribute an electron to the external circuit. The integral is made over all energies relevant to the solar spectrum. Since these parameters depend on the illumination it is necessary to define standard test conditions in order to compare different solar cells. These standard conditions are a temperature of 25 ℃, an irradiation power density of $1000\ W/m^2$ and $AM1.5$. The *air-mass* parameter $AM1.5$ describes the spectrum of the sunlight with an attenuation corresponding to the sun at an elevation of 42 °, or travel length for the sun rays through the atmosphere of 1.5 times that of the sun being directly overhead.

Now applying an external load to the solar cell will give a potential in between the extremes above; that is the voltage V is between zero and V_{OC}. This voltage gives rise to a current called the *dark current* and defined by the diode equation (2.29):

$$I_{dark}(V) = I_0\left(e^{\frac{qV}{nkT}} - 1\right) \tag{2.36}$$

The total current is then given by the difference between the dark current and the photo-generated, short-circuit, current.

$$I(V) = I_{dark}(V) - I_{SC} \tag{2.37}$$

Figure 11 shows the IV-curve for the dark current and for the total current under illumination. Generated power from the solar cell is the product of the current and the voltage $P = I(V) * V$. The signs of the quantities above imply that the negative power in the fourth quadrant is corresponding to production of power in the cell. As a side note it is worth mentioning that this sign convention is often reversed in the solar cell community to have positive values for power production and the graphs of interest in the first quadrant. Minimizing the power function gives the maximum power output for the cell at P_{max} for I_{mp} and V_{mp}. The maximum power point is found at the voltage that fills the largest fraction of the area under the IV curve. This is illustrated by the shaded region. In Figure 11, the shape of the IV-curve is given by the ideal diode equation, but a higher ideality factor will severely limit the maximum power output, as will parasitic resistances. A measure for the squareness of the

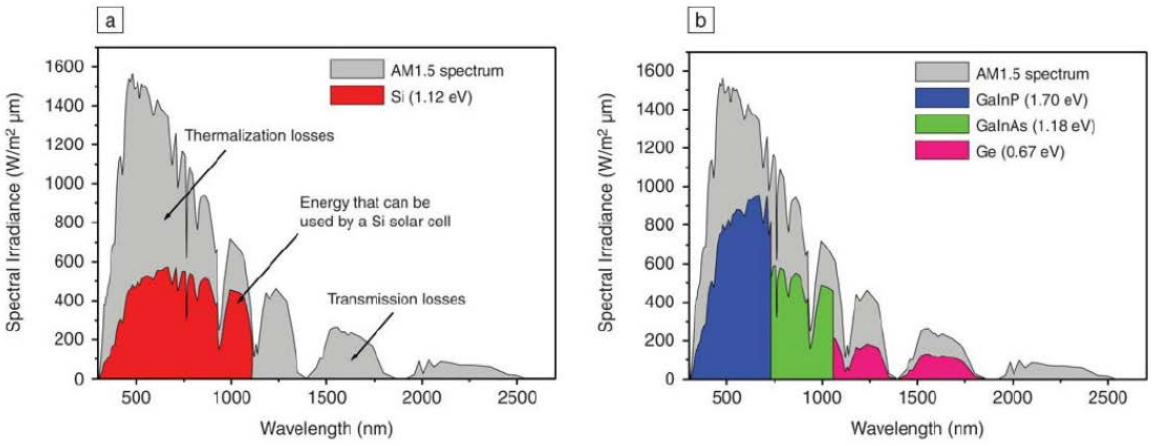

Figure 12 – Solar spectrum with AM1.5 attenuation. Energy utilization achieved with a single junction silicon solar cell (a), and a triple junction GaInP/GaInAs/Ge (b). The figure is reproduced from [25].

IV-curve is called the fill factor FF and defined as the ratio of the maximum power output to the hypothetical power of the open circuit voltage and short circuit current:

$$FF = \frac{I_m V_m}{I_{SC} V_{OC}} \tag{2.38}$$

Another important quality measure for the solar cell is the efficiency η. This is defined as the ratio of the maximum power output to the power associated with the incident light P_s.

$$\eta = \frac{I_m V_m}{P_s} \tag{2.39}$$

2.6.3 SOLAR SPECTRUM AND THEORETICAL OUTPUT

The basic silicon solar cell discussed above has a theoretical maximum efficiency of about 30 % at the standard test conditions. This limit was calculated in 1961 by Shockley and Queisser [24] and is called the detailed balance limit; also known as the Shockley-Queisser limit. The calculation takes into account the solar spectrum as in the standard conditions, the band gap, and an assumption that only radiative recombination occurs by modeling the solar cell as a black body.

With a band gap of 1.12 eV at 300 K silicon absorbs photons only if they have higher energy than this, thus excluding much of the low frequency infrared part of the spectrum. In addition the excess energy above 1.12 eV for higher energy photons is quickly lost after excitation as the electrons relax to the conduction band edge. This energy loss causes heating of the material and the process is called thermalization. Figure 12a shows the $AM1.5$ solar spectrum, and the red overlay shows the fraction that is utilized by an ideal silicon solar cell. The efficiency of real cells based on different technologies is tracked by NREL, the National Renewable Energy Laboratory in USA [26]. This is shown in the plot in Figure 13. Single crystalline silicon has a record efficiency of 25 %, where the difference from the theoretical limit mainly comes from reflection and recombination. It is however clear from the figure that there exist technologies with significantly higher efficiency; these are discussed in the next subsection.

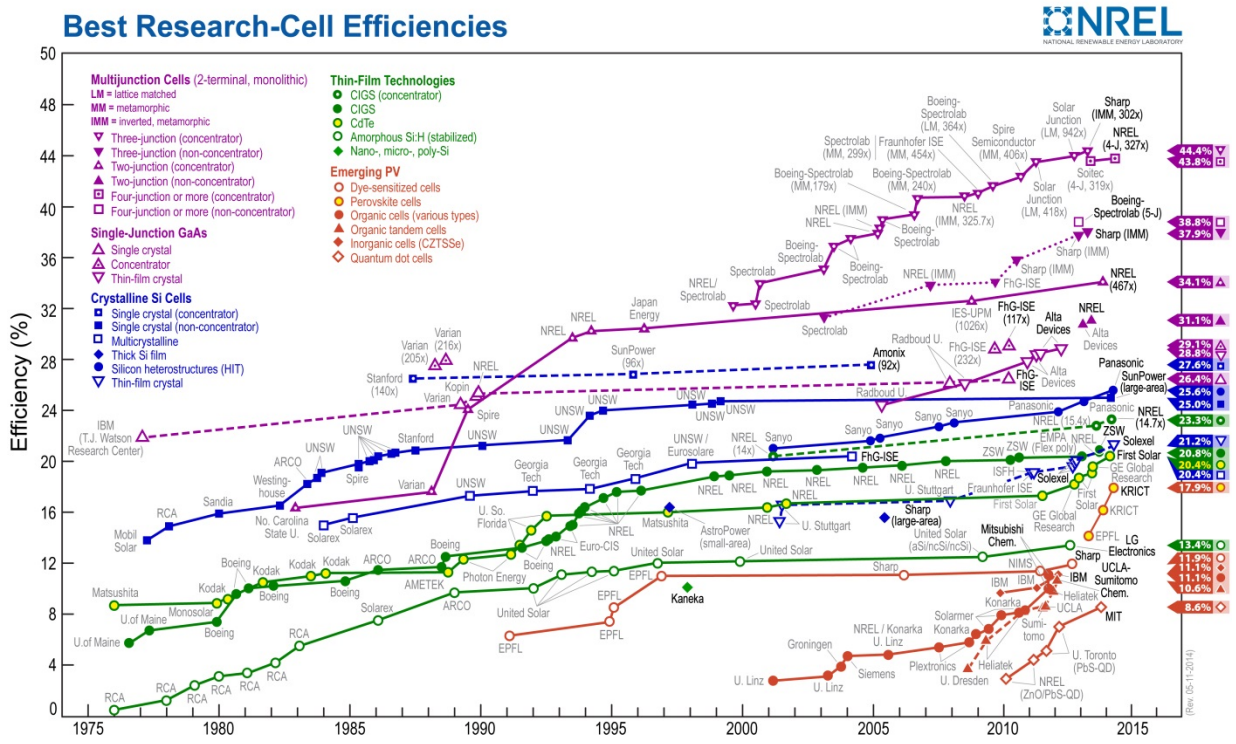

Figure 13 – NREL's efficiency chart for different solar cell technologies. [26]

It is also common to see efficiencies given for concentrated sunlight. Concentration can be achieved by mirrors or lenses, and if the temperature is controlled, higher efficiencies can be achieved due to black body considerations. The maximum theoretical concentration is close to 46000, corresponding to radiation with the suns intensity from the whole hemisphere above the cell. However practical concentrations are in the order of a few hundred.

2.6.4 TANDEM CELLS

By stacking multiple junctions with different band gaps it is possible to exploit more of the energy provided in the solar spectrum, such stacks are called tandem solar cells. Utilization of the spectrum by a triple junction solar cell is seen in Figure 12b. The idea is that the top junction absorbs the highest energy radiation while being transparent to light with longer wavelength. Subsequent junctions work similarly, taking portions of the spectrum. This way a smaller part of the total incoming light is lost through thermalization. Two different arrangements of these junctions are possible. The first alternative is to have separated junctions with individual connections to the external circuit. This would give the best output, but is difficult to achieve while keeping transparency. The second alternative is to make so called tunneling junctions. Then the junctions are in electrical series connection with each other through a very highly doped interface region that mimics Ohmic behavior by tunneling the carriers through a thin junction. This second solution is easier to achieve, but limits the power output as the current must be constant throughout the cell.

The theoretical maximum efficiency can be calculated for these cells as well, Table 1 is adapted from De Vos [27] and shows values for tandem cells with up to four junctions in series under un-concentrated sunlight. The mathematical limit for a cell with an infinite amount of junctions is also included; this translates to a continuously decreasing band gap junction with ideal extraction of the

carriers without relaxation. For a cell with three junctions the maximum is found to be 49 % for un-concentrated light. With concentrated light the maximum increase to 63 %. Going back to experimental results it is clear from Figure 13 that Sharp currently leads the efficiency race with a demonstrated efficiency of 44.4 % for a three-junction cell under concentrated light. This cell is based on III-V compound semiconductors, referring to the group of the atoms in the periodic table. The junctions in the cell are InGaP, GaAs, and InGaAs, going from high to low band gap respectively [28]. This material system is convenient as the band gap can be tuned by the composition, while the lattice mismatch is kept to a minimum. It must be emphasized though that this cell is only a research cell at $4 * 4\ mm$ in size.

Table 1 – Theoretical maximum efficiency for tandem solar cells with n junctions, and their optimal band gap values. These values are for solar cells under un-concentrated illumination. Table adapted from [27].

n	η (%)	$E_{g1}(eV)$	$E_{g2}(eV)$	$E_{g3}(eV)$	$E_{g4}(eV)$
1	30	1.3	-	-	-
2	42	1.9	1.0	-	-
3	49	2.3	1.4	0.8	-
4	53	2.6	1.8	1.2	0.8
∞	68		Continuous		

2.6.5 Transparent Conducting Oxides

Regardless the material system, any solar cell must have contacts on both sides of the pn-junction in order to extract the electrical current. The backside contact can cover the whole cell and the only demand is that a good Ohmic contact can be made with a metallurgical good interface to avoid unnecessary recombination. As mentioned the design of the front side contact is a trade-off between light reaching the active pn-junction and the ability to collect the generated carriers. On the basic silicon cell the grid of front contacts might cover up to 10 % of the total area, which is of course detrimental to the overall cell output. Contacts buried in grooves were already seen in Figure 9 to reduce the area coverage.

Another solution is to search for materials that can be used on the surface combining electrical conductivity and transparency. A class of materials labelled as Transparent Conducting Oxides (TCOs) complies with these demands. Common to TCOs is a high band gap that allows transparency, and the ability to be doped to a degenerate state to give good electrical conductivity. Degenerate doping means to dope the material so heavily that the dopant level splits into a sub-band that overlap with the band edge, providing a high and metal-like conductivity. The first example of a TCO was described in 1907 by Bädecker, resulting from oxidation of a sputtered cadmium film. Since then, this material class has been of interest with respect to a range of technologies, including opto-electronics as well as heated and heat reflecting windows. Since the development of flat screen technologies, Indium Tin Oxide (ITO) has been the benchmark material for TCOs. ITO is routinely produced with resistivity in the range of $1 - 2 * 10^{-4}\ \Omega\ cm$ by several deposition techniques [29] [30]. The lowest reported value is $7.7 * 10^{-5}\ \Omega\ cm$ on a sample with optical transmittance of 85 % in the visible range of wavelengths from $340\ nm$ to $780\ nm$ [31]. With a mixture of 90 % indium oxide (In_2O_3) and 10 % tin oxide (SnO_2) there is however one big disadvantage with this material. Indium scarcity

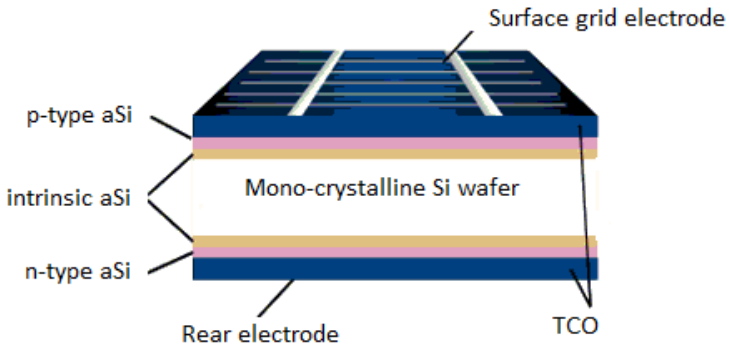

Figure 14 – Schematic of the HIT solar cell structure, adapted from [35].

drives the prices on this metal, and it is generally believed that supplies will end in the not too far future. Therefore, considerable research activity has been focused on finding new material systems to replace ITO. Carrier concentrations on the order of $10^{20}\ cm^{-3}$ and band gap over 3 eV are considered necessary [30]. Fluorine tin oxide is one option; with lower price and better thermal and chemical stability it has taken some of the market from ITO in solar cells despite poorer performance [32]. Zinc oxide is another competitor in this race, already incorporated in thin film solar cells based on the $Cu(In, Ga)Se_2$ (CIGS) material system [33].

For solar cell use, at least two options for utilizing the properties of TCOs are possible. The first is to facilitate a thin film of the TCO on top of a regular solar cell forming an Ohmic contact to the emitter. This way the metal contacts can be eliminated, or at least placed with a reduced density and area coverage. The second option is to produce an n-type TCO that simultaneously acts as the emitter itself.

2.6.6 HIT

While the afore-mentioned efficiency of the standard silicon solar cell has stagnated at 25 % heterojunction cells have in the recent years approached, and surpassed this level. The *Heterojunction with Intrinsic Thin-layer* (HIT) structure was presented by researchers at Sanyo in 1991 [34], and it has recently reached an efficiency of 25.6 % [6], as seen in the NREL chart of Figure 13. The efficiency increase has been attributed to reduction of recombination on the surface. The HIT structure is a combination of the bulk and thin film technologies as it utilize a crystalline base with thin deposited amorphous layers of intrinsic buffer and an n-type emitter. The use of TCOs is also central to this cell design. An amorphous emitter allows a transition from the crystalline Si to the TCO with reduced challenges of lattice mismatch. Applying an intrinsic layer between the emitter and base allows a wider depletion region in the junction. This is needed as the diffusion length is low in amorphous materials compared to crystalline and generated electron-hole pairs must be separated close to where they were generated. The intrinsic layer must, however, not be too wide, as series resistance might become large and the electric field reduced by charged defects. Texturizing both the front and backside of the cell gives good light trapping properties and allows production with thinner wafers. This, along with low temperature production processes, reduces the production cost compared to other technologies.

2.7 SCOPE OF THE WORK

Embracing the HIT structure for solar cells and the idea of ZnO as TCO, the scope of this work is to investigate the ZnO/Si heterojunction with respect to electrical properties and interface quality. The goal is to evaluate the influence of different thicknesses and compositions of the intrinsic buffer layer. The compositional variations will be done to engineer the band structure, and in practice this is done using amorphous Si and additions of Ge and C to decrease and increase the band gap, respectively.

2.8 PREVIOUS WORK

In this section follows a literature review of some previous knowledge on zinc oxide and the zinc oxide-silicon heterojunction.

2.8.1 ZINC OXIDE PROPERTIES

Fundamental properties of ZnO are summarized by Janotti and Van de Walle [15], Özgür et al. [36] and Liu et al. [32]. These reviews are the basis for the present subsection. Crystalline ZnO with the wurtzite structure exhibits 'native' n-type conductivity. This has been attributed to intrinsic defects in the material such as oxygen vacancies (V_O) and zinc interstitials (Zn_i). However theoretical and experimental studies of these defects amongst others have shown poor coherence between the conductivity and defect properties. Oxygen vacancies for example are found to contribute little to the conductivity as the donor level is too deep in the band gap, even though the low formation energy implies relatively high concentration. Unintentional hydrogen doping is found to contribute with shallow donor levels both for interstitial hydrogen and substitutional hydrogen on oxygen sites. Combined with the fact that hydrogen is present in almost all growth techniques this has gained acceptance as one explanation for the n-type conductivity. Additional n-type doping is easily achievable by group III dopants and other elements as substituents on the zinc sites. Aluminum and Gallium doped ZnO are frequently used, and abbreviated AZO and GZO, respectively. AZO will be used in the work in this thesis. P-type doping on the other hand is difficult, and although significant research resources have been invested, the results are still unstable and non-reproducible. Nitrogen is regarded most likely to be a successful acceptor. The challenge is that even though it is not the intrinsic defects that contribute n-type conductivity they may inhibit p-type conductivity by compensating the acceptor doping through deep levels. This lack of successful p-type doping is clearly a restriction for applications where a homojunction is sought after.

The next important property of ZnO is its transparency to visible light enabled by the wide band gap of 3.37 eV. This corresponds to a wavelength of 0.37 μm, which is in the ultra violet range and precludes absorption of lower energy light. For degenerate doping the transparency boundary may move to even higher energy by the Burstein-Moss effect. This happens when the Fermi level moves into the conduction band and the lower part of the conduction band becomes fully occupied. Kim et al. [37] has studied the shift for Ga doped films. A good fit to theory was achieved when also accounting for band gap narrowing, due to many body effects, and non-parabolic bands. For a film of 185 nm thickness and with $n = 4.94 * 10^{20}\ cm^{-3}$ a 0.28 eV shift was reported. A similar account is also given by Abdolahzadeh et al. [38], although slightly lower values of 0.2 eV for comparable

carrier concentrations are obtained. This corresponds well to experimental values from sputtered samples by Oh et al. [39].

Reduced transmittance is seen also for low energies. This is due to plasmon resonance in the electron gas of the conduction band. The plasmon frequency comes from a collective oscillation of the conduction electron gas, and photons with lower frequency are reflected from the material [10]. The plasmon frequency is also dependent on the carrier concentration. A shift to higher energies is the result for this boundary as well with increased doping. With higher magnitude than for the high energy boundary, the effect is a narrowing of the transmitted spectrum with higher doping of the ZnO. This implies that with respect to doping a trade-off must be made between the transparency and the conductivity of the material.

2.8.2 THIN FILMS OF ZINC OXIDE

Thin films of ZnO can be deposited in a number of ways, resulting in both polycrystalline and epitaxial films. Polycrystalline films can be produced with cheap methods such as spray pyrolysis and sol-gel, while epitaxial films can be achieved with more sophisticated methods as Pulsed Laser Deposition (PLD), Chemical Vapor Deposition (CVD) and Molecular Beam Epitaxy (MBE). Production of thin films by sputtering is another alternative; this typically yields polycrystalline films with a columnar structure. However, the control of composition and uniformity is better than with the cheapest methods, and cost and scalability are the advantages compared to the other advanced methods mentioned.

The lowest resistivities and highest transmittance in ZnO films are found to be comparable to ITO when produced with PLD. With AZO, film resistivity of $8.54 * 10^{-5}\ \Omega\ cm$ and transmittance of 88 % in the visible specter has been achieved [40]. GZO films are in the same range with resistivity $8.12 * 10^{-5}\ \Omega\ cm$ and transmittance of 90 % in the visible range as synthesized by Park et al. [41]. For sputtered samples Minami et al. [42] reported $3.69 * 10^{-4}\ \Omega\ cm$ with mobility $29.7\ cm^2/Vs$ and a carrier concentration of $5.7 * 10^{20}\ cm^{-3}$ achieved in $500\ nm$ films. Similar values are also reported elsewhere [43-46].

To achieve a low resistivity, both high mobility and high carrier concentration are needed. Ellmer [47] outlines a limit for the resistivity considering that very high doping gives increased scattering of conduction electrons on the impurity ions thus ultimately reducing the mobility.

2.8.3 PROPERTIES OF THE ZINC OXIDE-SILICON INTERFACE

Some examples of heterojunctions between ZnO and Si exist in the literature, focusing both on applications in solar cells and in photodiodes in the UV range.

Zink oxide films deposited on silicon by both sputtering and Atomic Layer Deposition (ALD) have recently been studied by colleagues here at the University of Oslo. The sputter deposited samples [48] were produced on p-type silicon wafers achieving a rectification of $3 - 4$ orders of magnitude. Heat treatments were done in the range $100 - 400$ ℃ and the samples were analyzed with IV, CV and DLTS. A reduction in the reverse saturation current and a slight increase in the rectification were found resulting from increasing annealing temperature. In forward bias the steepest IV curves was

found for the low temperature anneals. There was however no exponential behavior before the 200 ℃ annealed sample, from where ideality factors of around 5 were found. This high value of ideality indicates junctions with ample defects. Increasing series resistance was observed with higher annealing temperature and attributed to formation of a silicon oxide (SiO_x with $x \leq 2$) layer at the interface. Such an interface layer is also reported elsewhere [49], and Afify et al. [50] suggested to include a thin film of ITO at the interface to suppress the oxidation of silicon. Through DLTS two different defect levels was found at 0.38 and 0.43 eV above the valence band. These were confirmed to be associated with the material interface, and labelled H(0.38) and H(0.43) with H indicating their hole trapping properties. Additional broad peaks in the DLTS spectra for temperatures $80 - 200\ K$ indicate extended defects at the interface. At low annealing temperature the H(0.38) peak is clear, while at intermediate temperatures the broad peak dominates. The H(0.43) peak becomes clear after 200 ℃ annealing, with increasing concentrations at higher temperatures.

The experiment with ALD deposition [51] was done in order to characterize the barrier height for majority carriers across the junctions using both n- and p-type silicon wafers. From this the work function of ZnO could be deduced. ALD was chosen as it is a gentle deposition technique producing good quality interfaces compared to other methods, such as sputtering. Transmission Electron Microscopy (TEM) images along with IV curves with ideality factors close to unity confirmed good junctions. The silicon oxide layer was found to be less than 0.4 nm in thickness. Then temperature resolved IV and CV measurements were used to determine the barrier heights as can be seen in Table 2. It can be seen that the work function is $\phi_{ZnO} = (4.65 \pm 0.1)\ eV$. The resulting band structure is reproduced in Figure 15.

Table 2 - Barrier heights and ZnO-work function for samples of ALD ZnO on n- and p-type Si. Table adapted from [51].

	$\phi_b^{IV}(eV)$	$\phi_{ZnO}^{IV}(eV)$	$\phi_b^{CV}(eV)$	$\phi_{ZnO}^{CV}(eV)$
$ZnO - nSi$	0.61	4.66	0.66	4.71
$ZnO - pSi$	0.52	4.65	0.58	4.59

Investigation of the design of ZnO-structures with respect to use as a solar cell has been done with simulations by Nawaz et al. [52]. The basic structure was a 10 nm thin film of doped ZnO on an intrinsic ZnO layer of thickness in the range $0 - 120\ nm$ produced on crystalline silicon. Aluminum was used for front and backside contacts. With n-type ZnO and p-type Si efficiencies up to 20 % is achievable, while high interface defect concentrations are found to decrease this number rapidly.

Photoresponse in experimental samples are reported using several deposition techniques. In samples deposited by a sol-gel process Mridha et al. [53] compared ZnO films of different thickness. With a 460 nm film the resulting junction showed rectification of $5.7 * 10^3$ at 5 V, an ideality factor of $n = 4.15$ and a barrier height of 0.82 V was extracted from current-voltage measurements.

H.Y. Kim et al. [54] showed photoresponse in sputtered structures with both n- and p-type silicon wafers. The best rectification was found in the n-ZnO/p-Si samples. This was explained by a significantly higher barrier height, 1 eV more than for the n-ZnO/n-Si samples. Different deposition temperatures was used and the best photoresponse resulted from the samples deposited at high

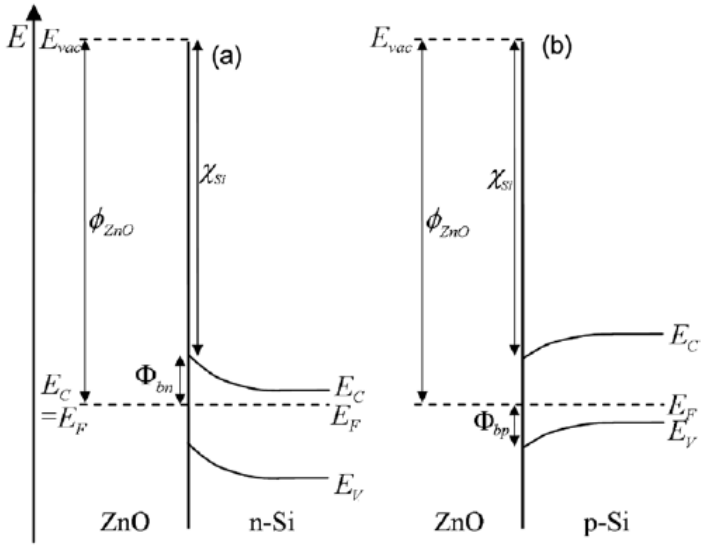

Figure 15 – Band structure of ZnO heterojunction to n-type (a) and p-type (b) silicon. The figure is taken from Quemener et al. [51]

temperature ($500\ °C$). An explanation for this was suggested involving higher transparency and film quality at this deposition temperature. The photoresponse gave a quantum efficiency of 32 % with a reverse bias of $5\ V$ and monochromatic illumination with a $670\ nm$ wavelength red laser.

Ben Ayadi et al. [55] recently produced a sputtered ZnO film on a p-type silicon substrate that was etched in order to achieve a porous surface. The porous surface is chosen to reduce problems related to lattice mismatch between the ZnO film and the substrate. Using the same sputtering parameters on glass substrate they report a resistivity of $1.56 * 10^{-4}\ \Omega\ cm$ and transmittance over 85 % in the visible spectrum. Applying an ITO layer and gold contacts the heterojunction under illumination gave a fill factor of 0.5 and efficiency of 5 %. This was resulting from an open circuit voltage $V_{OC} = 475\ mV$ and a short circuit current $I_{SC} = 21\ mA/cm^2$.

With two orders of magnitude rectification with $1\ V$ biasing J. Kim et al. [56] achieved an ideality factor of 1.19. Under illumination they got $V_{OC} = 321\ mV$ and $I_{SC} = 15.64\ mA/cm^2$, thus demonstrating the possibility for photovoltaic devices also in a junction between AZO and n-type silicon.

Sali et al. [57] has deposited various doped and undoped films of ZnO on a-Si:H/c-Si heterojunctions. Good transmittance of and low resistivity is reported in the aluminum doped samples, but a high ideality factor of 3.77 was reported and attributed to defects.

2.8.4 Band gap engineering

Band gap engineering in the ZnO-silicon heterostructure is possible on both sides. In ZnO the band gap can be increased up to 4 eV by alloying with magnesium oxide up to a concentration of 33 %. Similarly, cadmium oxide reduces the band gap down to 2.3 eV, but with lower concentration. Both magnesium- and cadmium oxide take the rock salt structure, so the limits of alloying comes from the

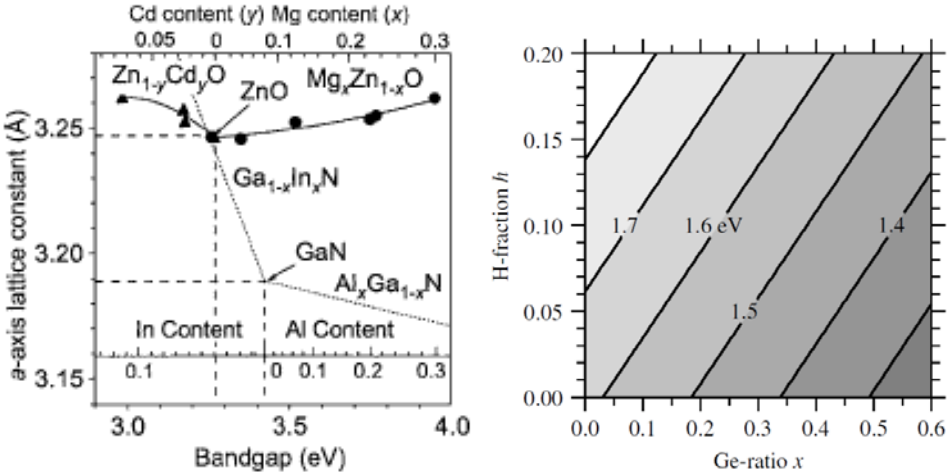

Figure 16 – To the left is a figure from Ozgur et al. [36] illustrating alloying in the ZnO system with CdO and MgO. To the right is shown the dependence of Ge alloying and hydrogen content in amorphous Si for the band gap, adapted from [60].

ZnO wurtzite structure's ability to embody these elements [15]. An illustration of the alloying is provided in Figure 16, adapted from [36].

Amorphous silicon typically has a band gap of around 1.8 eV while different deposition techniques can give some variation, especially considering different hydrogen content. As can be seen in Figure 16 alloying with germanium also allows tailoring of the band gap to lower values. Similarly, carbon can be used to increase the band gap. [58] [59].

PART II: EXPERIMENTAL METHODS AND SIMULATION

3 SYNTHESIS TECHNIQUES

In this chapter the relevant methods for sample synthesis are presented. The deposition techniques sputter deposition, Plasma Enhanced Chemical Vapor Deposition (PECVD) and electron beam evaporation (e-beam) are introduced, based on the work by Campbell [61].

3.1 SPUTTER DEPOSITION

The word sputtering describes the process when an accelerated ion which incident on a surface transfer momentum to the material, and thereby eject atoms or molecules from it. This effect is utilized in several processing and analysis techniques. Sputtering can be used for dry etching, which involves controlled physical removal of layers of atoms, and the advantage is its non-selectivity in terms of material that is etched. This controlled removal rate and non-selectivity is also needed in characterization methods with depth profiling such as Secondary Ion Mass Spectrometry (SIMS) and Auger Electron Spectroscopy (AES). In the following, the term sputtering refers to the sputter deposition. This is the primary deposition technique used in this work, and involves material being sputtered off of a target to then be deposited as a thin film on a substrate.

Advantages with sputter deposition include the ability to deposit material at a low substrate temperature, with good adhesion and inflicting little radiation damage at least compared to e-beam evaporation. Additionally, it is well suited to deposit alloys and compounds. These among properties others make it a widely used technique in the semiconductor industry, optics and for production of digital storage media. An illustration of a sputter deposition setup is shown in Figure 17. The basic feature of this setup is a vacuum chamber, where plasma is initiated between two electrodes. The cathode holds the target, while the substrate is on the anode. Successful sputter deposition demands close control over a series of physical parameters. A stable plasma must be maintained to provide the ions, an electric field must be present to accelerate the ions towards the target, and sputtered material must be transported from target to substrate. On the surface the conditions must allow adsorption and diffusion to achieve the desired structure and morphology. In the following subsections these topics will be discussed in more detail.

3.1.1 PLASMA PROPERTIES

A plasma is a gas where some fraction of the atoms is ionized. If the plasma is produced by an electric field it is known as a glow discharge. This name comes from the relaxation of atoms that has been excited, but not completely ionized, as it creates a characteristic glow. Initiation of the plasma can be done with a capacitor discharge or filament, partly ionizing the gas. With an applied electric field electrons and ions are then accelerated towards the electrodes. Collisions with atoms result in further ionization, and if this happens at a rate equal to the rate of recombination the plasma will be self-

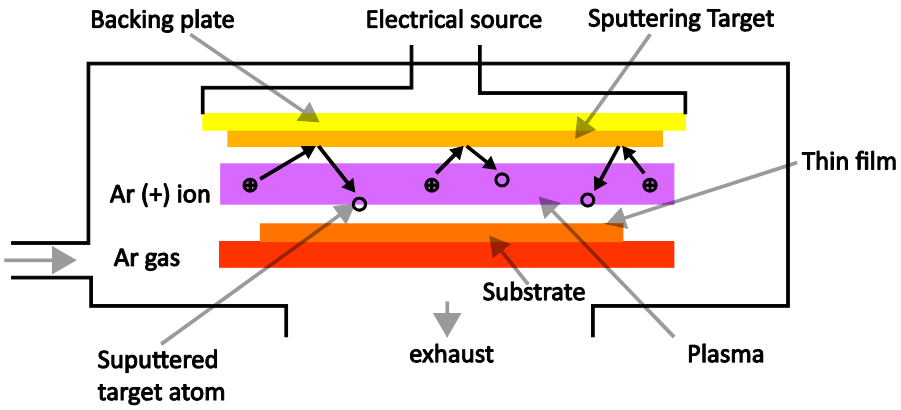

Figure 17 – Schematic illustration of the sputter deposition chamber. The sputtering target at the top is the cathode, and the substrate comprises the anode. The glow discharge is implied by the violet region with ionized argon atoms. This figure was adapted from [62].

sustained. A low pressure is needed to enable the charged species to be sufficiently accelerated to ionize atoms, but not too low as this would lead to too few collisions.

In between the electrodes several different regions result from the interaction between the charged particles, the electric field and the gas atoms. Effects of these interactions are illustrated in Figure 18. From the vicinity of the cathode electrons are quickly accelerated towards the anode. The region close to the cathode is thus depleted of electrons, and a positive charge builds up. As the electrons gain energy they are first able to excite the atoms, creating the afore-mentioned glow after a dark area close to the cathode known as Crooke's dark space. Even higher energy allows complete ionization and in the region known as the Faraday dark space this effect dominates. The positive ions created here partially shield the region closer to the anode. Electrons that have lost their kinetic energy in an ionization event will again be accelerated towards the anode, but in a lower field this results in excitation rather than ionization in the positive column. The anode acts as an electron sink and effectively depletes the immediate vicinity of electrons thus quenching the glow. The ions in the plasma are accelerated towards the cathode. Under the right circumstances the ions gather sufficient kinetic energy to enable sputtering of the target cathode. This process is accompanied by the release of secondary electrons which again is accelerated away, sustaining the plasma in the chamber.

3.1.2 SPUTTERING ACTION

In sputter deposition setups a high vacuum is the starting point before the plasma is initiated. This is done to control the plasma constituents and avoid contaminating the deposited film. Usually an inert gas is used for the plasma as it will not react with the sputtered material or the substrate. The most efficient momentum transfer and thus sputtering occurs if the mass of the ions match that of the target atoms. With these criteria, argon is a common choice for sputtering of most semiconductors, and it is used also in the present work. It is possible to use reactive gases too, where a reaction takes place between the sputtered material and the gas to produce the deposited material.

A wide range of ion energies result in sputtering action. For energies outside this range other interactions with the surface dominate. At low energy, typically less than 10 eV, ions are more likely to adsorb on the surface, create surface damage or simply be reflected (back-scattered). At too high

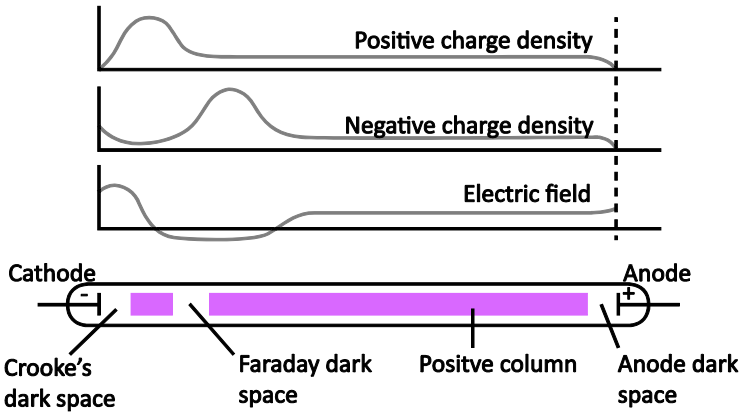

Figure 18 – The figure is adapted from Campbell [61]. Graphs at the top illustrate the charge densities and the electric field between the electrodes. The dark spaces and regions with glow are illustrated in the bottom part.

energies, most of the ions are implanted in the bulk of the material thus reducing the amount of sputtered particles. This typically applies to ion energies higher than 10 keV. For a qualitative understanding, the interaction between incident ions and target atoms can be considered as elastic collisions between spheres. But for a quantitative analysis a more thorough inspection of the coupled effect of bond breaking, electronic excitation and physical displacement must be performed.

3.1.3 RF SPUTTERING

The plasma behavior discussed above, with constant potential on the electrodes is well suited for conducting substrates and targets. It is characterized by the direct current going from anode to cathode and sputtering under these conditions is known as DC sputtering. In the case of insulating materials on the electrodes, charge would build up and choke the plasma. This is because the emission of secondary electrons from the cathode would reduce its negative charge, and the anode's positive charge would be compensated by the collection of electrons. Alternating the polarity of the potential on the electrodes is a way to circumvent this problem. This is done with a radio frequency potential and thus abbreviated RF sputtering. With their low mass, electrons respond instantaneously to this altering electrical field, thus striking both target and substrate and eliminating the large charge build-up. As opposed to the electrons, the heavy ions' paths do not change with the radio frequency. Directing the ions towards the target, and avoid sputtering of the substrate, can be done by superimposing a direct potential difference between the two electrodes.

3.1.4 YIELD AND MORPHOLOGY

The sputter yield, S, is a figure of merit, defined as the ratio N_e/N_i where N_e is the number of ejected atoms and N_i is the number of incident ions. Combined with the flux of ions to the target (J_{ion}), the transport efficiency to the substrate (E_T) and the number density of the sputtered particles (ρ/m), the deposition rate can be calculated from $R_d = (J_{ion} * S * E_T)/(\rho/m)$. For practical purposes, however, the deposition rate is determined experimentally.

By utilizing High Density Plasmas (HDP) the deposition rate increases due to the high ion concentration. One way to achieve HDP is by introducing magnetic fields with so called magnetron sputtering. In a magnetic field $\boldsymbol{B}$ particles with a charge q and velocity $\boldsymbol{v}$ are subject to the Lorentz

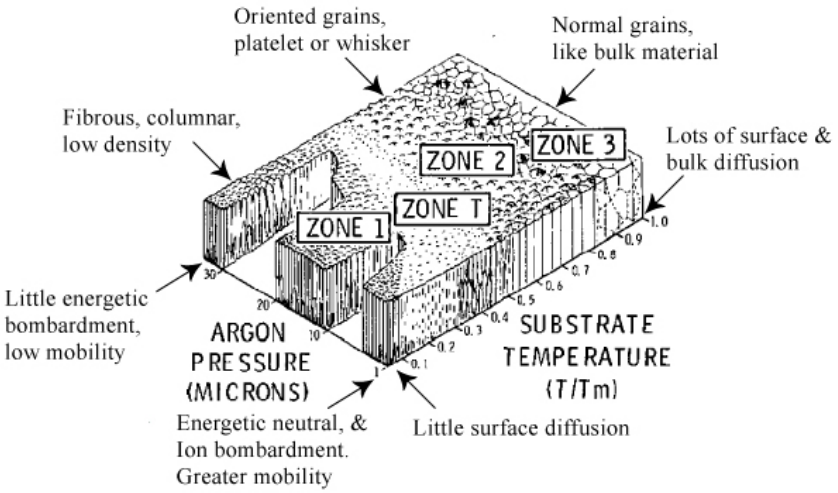

Figure 19 – Thornton's [63] zone model is shown in this figure, with labels as added by [64].

force $F = q\boldsymbol{v} \times \boldsymbol{B}$. This results in a circular motion of the particles. By tuning the magnitude of the field it is possible to give electrons a significantly increased travel length through the plasma, while ions with their higher mass only experience minor deviations. From the increased travel length for electrons follows an increase in the probability of ionization and thus the density of ions. An added advantage is that it is possible produce the plasma at lower chamber pressures.

When a sputtered atom reaches the surface of the substrate it carries 10-50 eV of kinetic energy, which is approximately two orders of magnitude more than for evaporation systems. This leads to comparably high surface mobility, long surface diffusion distances and thus good step coverage. The diffusion of the individual atoms on the surface stops when nuclei of critical size are produced. The nuclei proceed to capture more atoms and create islands on the surface. Eventually, islands merge and form a continuous film. The morphology of the deposited film is strongly dependent on the mechanisms and rates mentioned, and can be controlled by altering the substrate temperature and the pressure. This can be seen in the illustration of the zone model in Figure 19, where T/T_M is the temperature normalized to the melting temperature of the deposited material. Ion energy is inversely proportional to the plasma pressure given on the other axis of this illustration. In the first zone low temperature and ion energy give poor surface mobility which results in amorphous and porous films. Fine grains and a smooth surface result upon transition into the T zone. With further increase in the temperature zone 2 gives columnar grains and a rougher surface. In zone 3 grain size increases further and the film resembles a polycrystalline bulk material.

3.2 PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION

Sputtering a material leads to formation of a vapor and subsequent deposition of a film through a purely physical process. Sputter deposition is therefore often characterized as a Physical Vapor Deposition (PVD) technique. In contrast, Chemical Vapor Deposition (CVD) techniques are based on

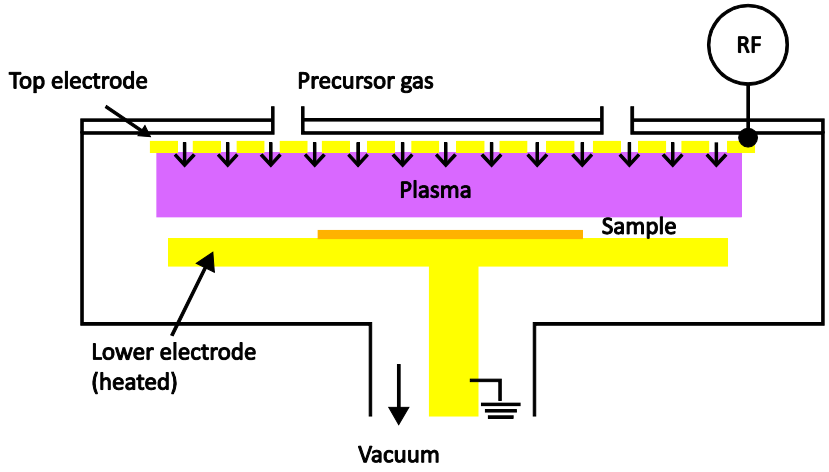

Figure 20 – A parallel plate PECVD setup is shown in this figure adapted from [65].

chemical reactions to produce the deposited material. A variety of different CVD methods exist, but they share some common features. The substrate is located in a chamber that is exposed to a gas flow carrying precursors for the deposited material. With some stimuli, e.g. heating, the precursors react close to the substrate surface. Usually several different species result from the precursors, including the reactants needed to deposit the desired material. Transport of these reactants to and on the surface takes place, followed by surface reactions. Then by-products of the precursors are swept away by the gas flow, leaving a film of the deposited material. Figure 20 shows a schematic of a parallel plate PECVD setup. The precursor gas is introduced to an initially evacuated chamber through a showerhead at the top. This showerhead also acts as one of the electrodes for the plasma. The other electrode holds the substrate, and the byproducts of the deposition are pumped out through the bottom of the chamber

To enable CVD at low temperatures, plasma can be used as the driving force for the chemical reactions. In the plasma the electrons quickly gain a high kinetic energy which enables dissociation of the precursors into more reactive species. RF plasmas are typically used, as PECVD are often used for insulating materials such as silicon dioxide (SiO_2). Different HDP techniques are applicable also in PECVD. Ion bombardment of the substrate surface can also be used to improve the quality of the film. Low energy ions give energy to the adsorbed molecules and atoms giving higher surface mobility and thus good step coverage. While this is not relevant to solar cells high aspect ratios are frequently encountered in the production of electronic devices. Some degree of sputtering can enable re-deposition and further increase the coverage along with the film quality.

3.3 ELECTRON BEAM EVAPORATION

Evaporation of atoms from a melted material gives an equilibrium vapor pressure largely dependent on the temperature. For evaporation suitable for deposition of thin films a vapor pressure of more than 10 $mtorr$ is considered necessary, for aluminum this is achieved at 1250 ℃. The evaporation gives a flux of atoms from the melt and if in a high vacuum chamber ($\sim 10^{-6}$ $torr$) the evaporated material will travel in a straight line from the melt. By placing substrates in a hemisphere above the melt a

homogeneous deposition rate proportional to the flux can be achieved over relatively large areas. Rotation of the samples in the hemisphere further improves the homogeneity. Measuring the resonance frequency of a quartz strip placed on this hemisphere among the samples allows accurate calculation of the deposited thickness in real time. This way the temperature and thus deposition rate can be adjusted during the deposition process.

Poor step coverage due to low surface mobility on the substrates is one drawback with this deposition technique. This can in some cases be an advantage for instance in a process called lift-off where a lithographic mask shades regions of the substrate. Material deposited on the mask is then removed with the mask as it is not in physical contact with the material deposited through the mask. It is also possible to deposit well defined patterns through a shadow mask simply pressed against, or in close vicinity of the substrates. A challenge is that alloys and compound materials might consist of elements with very different vapor pressures giving different stoichiometry in the deposited material compared to the melt. The latter can in some cases be circumvented by using multiple crucibles with different heating.

Several different methods exist for heating the crucibles, with resistive heating being the simplest concept. This, however, implies heating both a filament and the crucible itself, in addition to the source material i.e. the charge. Evaporation from the filament and crucible may lead to contamination of the deposited film. Inductive heating of the crucible can be done with cooling of the coil; this eliminates the filament contamination while the crucible contamination persists. Heating the charge with a beam of high energy electrons avoid also the crucible contamination. The electron beam (e-beam) is provided by an electron gun, e.g. a tungsten filament, where electrons are boiled off due to high biasing and current flow. For this heating technique the melt is self-contained in the charge; the heating is localized to the narrow area of incident electrons. Some contaminants from the filament of the electron gun might be expected, but this can be minimized by placing the gun underneath the crucible and directing the electron beam with a magnetic field. Radiation damage of the substrate is an issue with this technique precluding its use for some technologies. This is to some extent a result of generation of x-rays upon relaxation of excited electrons in the melt.

4 SAMPLE PREPARATION

Details and parameters for the production of the samples used in this work follow in the present chapter; a schematic of the device structures is shown in Figure 21. The steps undertaken in the synthesis of the samples is provided in the block diagram in Figure 22. The samples were made in two batches as indicated in Figure 22. The second batch, with sputtered buffers, was split into four prior to contact deposition. Of these, one was kept *As Deposited* (AD) and the rest was later subject to annealing at 300, 400, and 500℃. From this a total of 64 different samples became subject for the electrical characterization discussed later. In the following presentation of results the samples are referred to by their buffer properties, i.e. thickness and material as well as the substrate type.

4.1 WAFERS AND PRE-DEPOSITION CLEANING

All combinations of buffer parameters used were applied to wafers of both n- and p-type with (1 0 0) surface orientation. The n-type wafer is from Ultrasil, with resistivity in the range $1 - 10\ \Omega\ cm$ and doping concentration $N_d \approx 1 * 10^{15}\ cm^{-3}$. The p-type wafer has slightly higher resistivity range, and $N_a \approx 9 * 10^{14}\ cm^{-3}$. Prior to deposition, all samples were cleaned in a bath of hydrofluoric acid (HF) and subsequently rinsed in water. The samples were blown dry with nitrogen (N_2) and inserted for vacuum pumping in the chamber of deposition, with a minimum of time delay.

4.2 SAMPLES WITH PECVD GROWN BUFFER LAYER

The first batch of samples is shown in the left string of the block diagram in Figure 22. Amorphous silicon was deposited with thickness of about 5, 10 and 20 nm, while one sample was left without this buffer layer. A *310 MKII* PECVD system from *Advanced Vacuum* was used for this deposition. The deposition was performed at 180 ℃ substrate temperature, with an RF power of 30 W, and a chamber pressure of 600 $mtorr$. The precursor gas was 2 % silane in nitrogen with a flow rate of 2000 $sccm$; the unit $sccm$ is an abbreviation for *Standard Cubic Centimeters per Minute*, and 1 $sccm$ thus corresponds to a flow of 1 cm^3/min for standard temperature and pressure conditions. Amorphous films with a band gap of $\sim$2.0 eV and low hydrogen content is anticipated. Avoiding hydrogenation, in contrast to what is common in these structures, is done for the structures to be comparable with those from sputtering. Hence, surface passivation by H is intentionally omitted. Deposition times used were 0: 37, 1: 15 and 2: 30 $min: s$, to yield 5, 10 and 20 nm film thicknesses.

After PECVD deposition of the buffer layers, all the samples were loaded into the sputtering equipment, a *Semicore Triaxis*, for collective deposition of aluminum doped zinc oxide (AZO). Evacuation of the chamber was done to a base pressure $5.8 * 10^{-7}\ torr$, and pre-sputtering with closed shutters was performed in order to remove any unwanted oxide and contamination from the target surfaces. The sample holder was heated to 400 ℃ and subject to a rotation of $\sim$12 rpm, in an

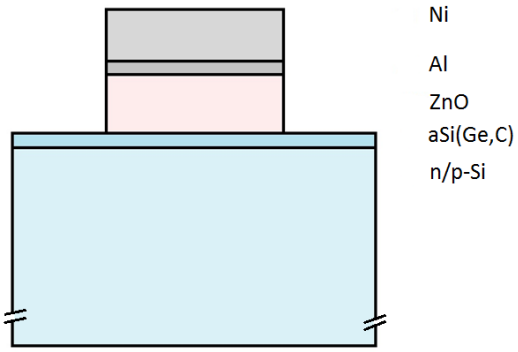

Figure 21 – Schematic representation of the sample structure.

argon gas flow of 70 $sccm$. The AZO film was deposited by co-sputtering with one aluminum target operated under DC conditions and a power of 7 W, and one RF ZnO target at 50 W. Giving a deposition rate of ~1.4 nm/min, two hours deposition time was used to produce a film of ~170 nm thickness. Visual inspection of the finished films revealed some color variations indicating non-homogeneity in the thickness. This was however considered not to pose a problem for the electrical characterization of the heterojunction as the film thickness is relatively large and the junction is one-sided into the silicon due to the high film doping concentration. For further discussion of the deposition parameters, the reader is referred to Schifano et al. [66].

Ohmic contacts to the ZnO were deposited with e-beam evaporation, using a Leybold L560 setup. At a pressure of 10^{-6} $mbar$ 10 nm of aluminum and then 100 nm of nickel was deposited at rates of 0.1 nm/s and 0.06 nm/s, respectively. The aluminum layer was used to form an Ohmic contact to ZnO, while nickel was applied on top of the aluminum to protect the contact during the subsequent etching of the ZnO layer. A shadow mask with a grid of circular openings was used for the deposition.

The etching step is done with HF diluted in water to a concentration of ~5 − 10 %. Dilution was increased during the treatment as some over-etching was observed for the first samples. The lateral etching of ZnO under the metal contacts is considered negligible in this context. The process is controlled visually and ended with thorough rinse in water before a nitrogen blow dry.

4.3 SAMPLES WITH SPUTTER DEPOSITED BUFFER LAYER

The principal difference between the two batches is that the PECVD step is eliminated in the second one, in order to vary the composition of the buffer layer. Both the buffer layer and the ZnO layer are deposited with sputtering in this second batch. Only 5 and 10 nm layers are produced, but three compositional variations are made. These are (i) pure silicon, (ii) silicon-germanium from a target with stoichiometry $Si_{0.85}Ge_{0.15}$, and (iii) silicon-carbide from a stoichiometric SiC target.

An additional advantage with this process is that it eliminates the need to break vacuum between the depositions thus minimizing the risk of oxide layer formation between the layers. On the other hand,

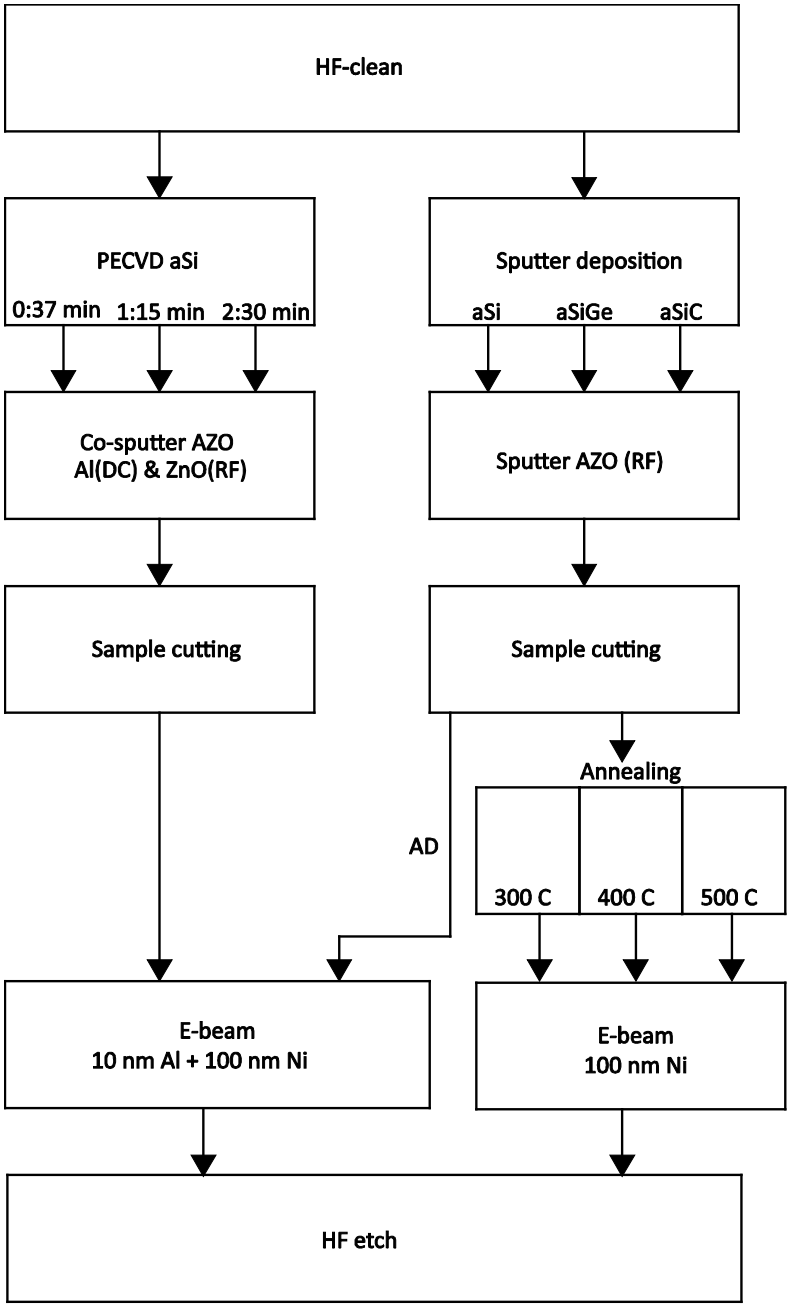

Figure 22 – Block diagram showing the steps undertaken in the preparation of the samples.

the quality of the PECVD grown buffer layer is expected to be higher than for the sputtered layer. However, a major objective of this work is to study the influence of surface composition of the buffer layer, rather than optimizing the process. For the same reason, passivation by H is omitted from the process.

Prior to deposition on the actual samples, the deposition rate of the buffer materials had to be determined. The rate for silicon was initially estimated from the silicon content achieved when co-sputtering with ZnO, as reported in [66]. A sputtered sample was prepared using a tape mask to create a step between the bare silicon wafer and the sputtered amorphous silicon. This step height was then

measured using a *Veeco Dektak 8* stylus profilometer to determine the thickness of the film. This procedure was repeated until a reliable rate could be established for a sufficiently thin film. In all cases these layers were deposited at room temperature with an RF power of 25 W. Moreover a base pressure in the range of 10^{-6} $torr$, argon flow of 70 $sccm$ and a $\sim$12 rpm rotation was used as above. In a separate deposition the buffer materials with germanium and carbon were also prepared in thicker layers on glass substrates for use in x-ray diffraction (XRD) structural analysis, resistivity measurements and optical characterization.

The deposition rates found resulted in deposition times of 10 and 20 minutes for the 5 and 10 nm layers of pure silicon. For $Si_{0.85}Ge_{0.15}$, deposition rate was slightly higher giving deposition time of 8 and 16 minutes, while SiC needed 20 and 40 minutes. This deposition was again done in pairs of n- and p-type Si wafers and the following AZO deposition done directly without breaking vacuum. In this case the AZO deposition was done with an AZO target with 5 % Al. The RF power used was 50 W and the sample holder was heated to 400 ℃, the other parameters were kept constant. For 5 nm silicon buffer samples, AZO films deposited at room temperature were also prepared (in addition to 400 ℃ ones). After sputtering, each of the deposited samples was split into four; one was directly deposited with metal contacts following the same procedure as for the first batch samples. The other three were subject to a post-deposition anneal at respectively 300, 400 and 500 ℃ for one hour. The annealing was carried out in a *GSL 1100X* oven made by *MTI corp.*, in a 1 $liter/min$ forming gas flow. The forming gas was a 90 % nitrogen and 10 % hydrogen blend. Hydrogen is assumed to easily diffuse through the ZnO and contribute to passivation of dangling bonds in the amorphous buffer layers. Parallel to the heat treatment of these samples the buffer samples on glass substrates were also annealed, although only at 400 ℃. Of each sample type one sample was annealed in the forming gas flow, and one in a pure nitrogen flow. The latter was done to simulate the heat treatment received during AZO deposition for the other samples.

After annealing the samples, metal contacts were deposited. This time the thin aluminum layer was omitted, to further reduce the etching observed on the metal contacts on the AD samples. Experience by others in the group suggest good Ohmic contacts with only nickel due to a very narrow barrier enabling tunneling of charge carriers into the heavily doped AZO film

4.4 PREPARATIONS FOR ILLUMINATION STUDY

A selection of samples was chosen for the investigation of photovoltaic action. These samples were cut in $6 * 6$ mm pieces with laser, to give clean cuts and avoid shunting of the deposited films around the edges. A Rofin scribing laser was used, which uses a green light laser with wavelength 532 nm. Using 26 A at 15 kHz and with a speed of 100 mm/s cutting through the samples was achieved with $\sim$400 executions. Similar cutting parameters were used for creating shadow-masks for deposition of front side contacts. The shadow-masks were made from a 380 μm silicon wafer, and with E-shaped slits. 0.5 mm thickness was used for the stem slit, and 0.2 mm for the arms, all lengths are 5 mm. Deposition of the front side contacts was done through the shadow mask, with e-beam deposition of aluminum with 150 nm thickness.

5 CHARACTERIZATION TECHNIQUES

In this chapter the relevant characterization techniques are reviewed. In accordance with the work done, electrical characterization will be emphasized the most.

5.1 CURRENT-VOLTAGE CHARACTERISTICS

Measuring current as function of voltage (IV) is directly relevant for the operation of the devices. Derivation of figures of merit such as ideality factor, barrier height and series resistance from these measurements is considered in this section. As a first approximation, in the experimental work the diodes will be assumed to follow the theory of Schottky diodes with reverse saturation current from thermionic emission across the barrier as described in section 2.5.1. The current-voltage relationship is then described by equation (2.29) and (2.32):

$$I(V) = I_0\left(e^{\frac{qV}{nkT}} - 1\right) = A^* A\, T^2 e^{-\frac{\phi_{bn,bp}^{IV}}{kT}}\left(e^{\frac{qV}{nkT}} - 1\right) \quad \textbf{(5.1)}$$

This approximation is based on the degenerate doping of the AZO film giving metal-like conduction. Both the barrier height to n-type (ϕ_{bn}) and p-type (ϕ_{bp}) substrates are related to the Fermi level, and the valence band of the ZnO is thus neglected. The superscript IV is used to separate the values deduced from IV measurements from those from CV measurements.

Comparison of the current in forward and reverse bias leads to the term rectification. This is normally referred to by how many orders of magnitude difference there is between the two for some choice of applied bias. High rectification is important in many applications. In the forward bias region it is ultimately limited by the series resistance, and discussed in a following subsection. The reverse bias region may also see large deviations from the ideal diode model resulting from defect rich interfaces or conduction mechanisms other than thermionic emission.

5.1.1 EXPONENTIAL FORWARD BIAS BEHAVIOR

When $V > 3kT/q$ the exponential term in equation (5.1) dominates, and the simplification $I(V) = I_0 e^{qV/nkT}$ holds. Rearranging and taking the logarithm yields:

$$\ln I(V) = \ln I_0 + \frac{qV}{nkT} \quad \textbf{(5.2)}$$

This allows a linear plot of $\ln I(V)$ versus V, or recognition of a linear region on a semilogatithmic plot of I versus V. For real devices, linearity is lost at higher forward bias when the series resistance becomes dominating. Hence, a linear fit is performed on the measurement data in the region with linear behavior. From the slope s the ideality factor can be deduced:

$$n = \frac{1}{s}\frac{q}{kT} = \frac{q}{kT}\left(\frac{d\ln I}{dV}\right)^{-1} \quad \textbf{(5.3)}$$

Extrapolation of the linear fitting to $V = 0$ gives the y-axis intercept equal to $\ln I_0$, and rearranging the thermionic emission expression yields the barrier height:

$$\phi_{bn,bp}^{IV} = kT \ln \frac{A^* A T^2}{I_0} \tag{5.4}$$

5.1.2 SERIES RESISTANCE

Series resistance is assumed to be Ohmic and contributes a prominent deviation of the IV characteristics expected from the diode equation at high currents. According to Ohms law the voltage drop over the series resistance R_S is $V_{R_S} = IR_S$. Equating the real diode with an ideal diode in series with a resistor, the voltage over the diode is reduced with the value over the resistor. Thus, $V_{diode} = V - IR_S$ where V is the applied bias. The diode equation becomes:

$$I(V) = I_0 \left(e^{\frac{q(V-IR_S)}{nkT}} - 1 \right) \tag{5.5}$$

A simple method for estimating the series resistance is the ΔV method. A current value is chosen in the region where the series resistance dominates, the corresponding voltage is compared to the voltage giving the same current in the ideal model so that:

$$R_S = \frac{\Delta V}{I} \tag{5.6}$$

An analytical solution to equation (5.6) is complicated by the current occurring on both sides. Banwell and Jayakumar [67] have derived such a solution, elaborated upon by Ortiz-Conde et al. [68]. This is based on the multivalued Lambert function $W_k(x)e^{W_k(x)} = x$:

$$I(V) = \frac{nkT}{R_S} W_0 \left[\frac{I_0 R_S}{nkT} e^{\frac{V + I_0 R_S}{nkT}} \right] - I_0 \tag{5.7}$$

Here W_0 is the principal branch of W_k yielding only real values and its solution is readily implemented in Matlab [69]. The advantage with this analytical model is that experimental data can be directly compared over all biases for any given series resistance. Both the above models have been used in this work.

It is possible, with highly resolved IV measurements, to calculate the series resistance using more of the forward bias data than in the first method. This is done calculating the conductance $g_d = dI/dV$. Plots of I/g_d versus I or g_d/I versus g_d should yield linear behavior where both ideality factor and series resistance can be deduced from the slopes and intercepts. [70]

5.2 CAPACITANCE-VOLTAGE CHARACTERISTICS

Assuming an asymmetrical pn-junction or a Schottky junction the depletion capacitance is given by equation (2.32). With measurements of the capacitance as function of applied reverse bias it is

possible to deduce values for the built in potential as well as the doping concentration of the low doped side. A typical derivation of these figures is done with a $1/C^2$ versus V-plot. This starts from rearranging the expression to:

$$\frac{1}{C^2} = \frac{2}{\varepsilon q\ A^2\ N_{d,a}} V_j \tag{5.8}$$

Remembering that $V_j = V_0 - V$ it is clear that a plot of $\frac{1}{C^2}$ as a function of V gives a straight line:

$$\frac{1}{C^2} = i + sV \tag{5.9}$$

where the negative slope s is inversely proportional to the doping concentration through $s = -2/(\varepsilon q\ A^2\ N_{d,a})$, and the intercept to the y-axis (i) reveals the built in voltage $V_0 = -i/s$. Being more stringent, a term kT/q must be added to the intercept value to account for the majority carrier tail (Debye tail) extending into the depletion region, which is ignored in the depletion approximation.

5.2.1 Determining barrier height from CV

As was the case for IV, the CV data from the junction between highly doped ZnO and silicon can be treated as that of a Schottky contact. The barrier height is the sum of the built in potential and the separation between the Fermi level and the majority carrier band plus the majority carrier tail-term mentioned:

$$\phi_{bn,bp}^{CV} = V_0 + \xi + \frac{kT}{q} \tag{5.10}$$

Here $\xi = E_C - E_F$ for n-type substrate and $\xi = E_F - E_V$ for p-type. Equations (2.5) through (2.7) are used to find ξ. The carrier concentrations are assumed equal to the doping concentrations found from the slope of the $1/C^2$ plot. For n-type substrates this gives

$$n_0 = N_d = N_C e^{-\frac{E_C - E_F}{kT}} = N_C e^{-\left(\frac{\xi}{kT}\right)} \tag{5.11}$$

$$\xi = -kT\ \ln\frac{N_d}{N_C} \tag{5.12}$$

5.3 Comparison of barrier heights from CV and IV

There are some inherent differences in the derivation of barrier height from CV and IV measurements that promote different results between the two. Thus, comparison of the data can help to understand the mechanisms at hand. For the IV data the barrier height is deduced from forward bias measurements, and is thus dependent on carrier transport across the junction. This makes it sensitive to any defect or mechanism that is not described by the diode equation or thermionic emission. For example, inhomogeneity in the barrier height will result in current flow preferentially in regions with low barriers. This is reflected by a lower barrier height deduced from these measurements. A reduced barrier height from IV measurements can also be expected accounting for image force lowering. This is the effect that a charge carrier approaching the interface from the semiconductor to the metal (or metal-like degenerate semiconductor) induces a mirror charge in the metal. An electron approaching

the interface deflects electrons in the metal, thus creating a positive mirror. This attracts the electron and the effect is a lowering of the barrier. On the other hand, none of the described mechanisms lower the barrier deduced from CV measurements. This is because the CV method depends on build-up of charges rather than the transport of these over the interface. With barrier height inhomogeneity the larger area properties will dominate the CV results.

Performing IV and CV measurements in a range of different temperatures allows further investigation of the junction properties. This is especially relevant for samples where the thermionic emission and ideal diode models are insufficient, as determined by high ideality factors in room temperature measurements. Also barrier height variations may be seen as function of temperature, as for example, where low barrier height patches in IV measurements become more favored at lower temperatures.

5.4 DEEP LEVEL TRANSIENT SPECTROSCOPY

Deep levels, also known as traps or recombination centers, were discussed in section 2.3.4. The characterization method used for deep levels in this work is known as Deep Level Transient Spectroscopy (DLTS), as introduced by Lang in 1974 [71]. The interest is on the trap signatures, as well as the concentration of different traps within the spectrum of energies in the band gap.

The term transient refers to a short time variation in some physical state. In deriving the emission rate in equation (2.18) equilibrium was assumed through the use of detailed balance. But as will be clear in this section, transients in occupancy coming from a non-equilibrium situation are central to the study of traps. Capacitance transients follow from the occupancy transients, and combined with a suitable weighting function this gives the DLTS signal as function of temperature $S(T)$. The present section is based on the work by Blood and Orton [17].

5.4.1 OCCUPANCY TRANSIENTS

The variation in trap occupancy with time $n_t(t)$ will be considered. With an initial concentration $n_t(t=0) = n_t(0)$ the time development of the concentration is found by solving equation (2.18):

$$n_t(t) = \frac{a}{a+b}N_t - \left(\frac{a}{a+b}\,N_t - n_t(0)\right)e^{-(a+b)t} \tag{5.13}$$

The development can be seen as an exponential relaxation from the initial concentration. The boundary at infinitely long time is a steady state concentration of $n_t(t=\infty) = n_t(\infty) = \frac{a}{a+b}N_t$ giving:

$$n_t(t) = n_t(\infty) - \big(n_t(\infty) - n_t(0)\big)e^{-\frac{t}{\tau}} \tag{5.14}$$

Here the reciprocal of the sum of the rates defines the time constant for the relaxation $\tau = (a+b)^{-1} = \big(e_n + c_n + e_p + c_p\big)^{-1}$. Depending on whether $n_t(0)$ is smaller or larger than $n_t(\infty)$ the direction of the relaxation varies. Simplifications of the above expression can be made for two special cases, when the traps are initially empty or initially full:

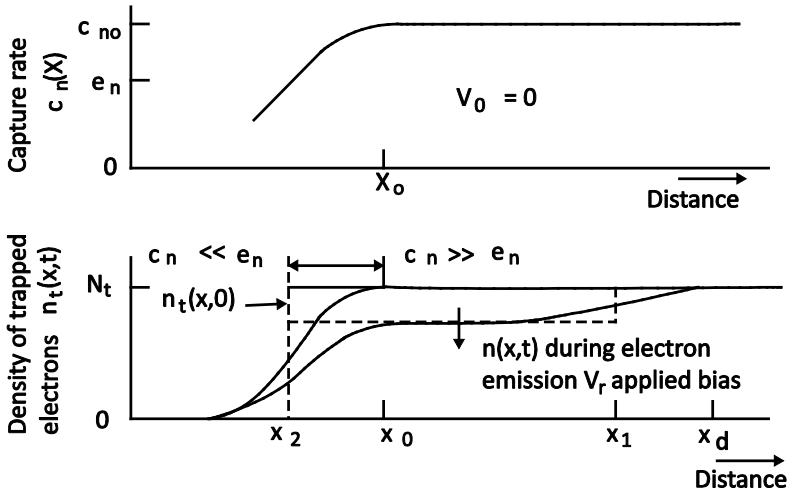

Figure 23 – The caputre rate is illustrated in the topmost graph, and seen to tail of into the depletion region. x_0 denotes the depletion region edge at zero bias. In the graph below is seen the density of trapped electrons for zero-bias (top curve) and a reverse bias extending the depletion region to x_d . Estimating the occupancy transitions as abrupt can be done by using x_2 and x_1 substituting x_0 and x_d. The figure is adapted from Blood and Orton [17].

$$n_t(0) = 0 \qquad n_t(t) = n_t(\infty)\left(1 - e^{-\frac{t}{\tau}}\right) \tag{5.15}$$

$$n_t(t) = N_t \qquad n_t(t) = \frac{a}{a+b}N_t + \frac{b}{a+b}N_t e^{-\frac{t}{\tau}} \tag{5.16}$$

Such assumptions are made with abrupt changes at the depletion region for eased understanding, although the more detailed picture involves transition regions of gradually changing occupancy at the depletion region edge. This is depicted in Figure 23.

5.4.2 Traps in depletion regions and capacitance response

It was discussed in section 2.3.4 that the emission rate from a trap is a function of temperature and can reveal the trap signature. In order to evaluate the emission rate of a trap it is preferable to isolate it from other processes. Depletion regions can be used to isolate the emission process. Both majority and minority carrier traps can be studied if choosing the right approach, however majority carriers are the focus in conventional DLTS studies.

A Schottky diode or an asymetrical pn-junction are typically utilized, since the depletion region mainly extends on one side of the junction, i.e. the low doped material is investigated. Taking a p^+n junction as the example, it is electron traps in the lightly doped n-type material that are studied. For a majority trap, in this case an electron trap, it is reasonable to assume that the capture and emission rates for minority carriers are significantly lower than, and thus negligible, the rates for the majority carriers. Further, as the depletion region has no free charge carriers also the capture rate of majority carriers is negligible, $c_n(n = 0) = 0$. Thus, the rate of change of electron occupancy of the trap is given only by the electron emission alone and equation (2.9) reduces to:

$$\frac{dn_t}{dt} = -e_n n_t \tag{5.17}$$

which integrates to:

$$n_t(t) = n_t(0)e^{-e_n(T)t} \tag{5.18}$$

Here the time constant of the relaxation is $\tau = -e_n(T)$ and the initial concentration of occupied traps is typically assumed to be given by completely full traps so that $n_t(0) = N_t$. This is reasonable since $c_n > e_n$ due to the relative position of the trap level and the Fermi level, which implies filling of the traps when there is no bias sustaining the depletion region.

Depletion capacitance is used to meassure the change in occupancy of the traps. Adopting the depletion approximation, the capacitance is given by equation (2.32), except the charge of traps must also be included. Thus, the charge density $\rho = qN_d$ must be replaced. An acceptor-like deep level contributes negative charge when occupied, and becomes neutral upon emission of electrons, the total charge density can be expressed $\rho(t) = q\big(N_d - n_t(t)\big)$. Conversely, an occupied donor-like deep level is neutral, and becomes positive when unoccupied giving the total charge density $\rho(t) = q\big(N_d + N_t - n_t(t)\big)$. In the following derivation, donor-like traps are assumed. Inserting the charge density into equation (2.32) give:

$$C(t) = C(\infty)\sqrt{1 - \frac{n_t(t)}{N_d + N_t}} \tag{5.19}$$

Here $C(\infty)$ represents the capacitance at reverse bias, after all the traps have emitted their electrons:

$$C(\infty) = A\sqrt{\frac{\varepsilon_r \varepsilon_0 q(N_d + N_t)}{2V_j}} \tag{5.20}$$

For trap concentrations much lower than the doping concentration (n_t , $N_t \ll N_d$) the capacitance changes $\Delta C(t) = C(\infty) - C(t)$ can be expressed as:

$$\frac{\Delta C(t)}{C(\infty)} = \frac{n_t(t)}{2N_d} \tag{5.21}$$

Using the approximation $f(x) = (1-x)^a \approx 1 - ax$, which is valid in the limit of small values of x, and inserting equation (5.18) into (5.21), it is clear that also the capacitance reflect the exponential relaxation of the occupancy.

$$\frac{\Delta C(t)}{C(\infty)} = \frac{N_t}{2N_d} e^{-e_n(T)t} \tag{5.22}$$

This relation is the basis of the DLTS method and its use will be discussed in the next subsection.

5.4.3 VOLTAGE PULSES AND CAPACITANCE TRANSIENTS

Pulsed biasing is used to fill traps and then study the emission rate in the depletion region, i.e. separating the capture process from the emission process. Figure 24a shows the biasing of the diode during the measurement. One cycle consists of two steps; first the traps are filled up by quenching the depletion region with a low reverse- or even forward bias. In this work a filling pulse duration

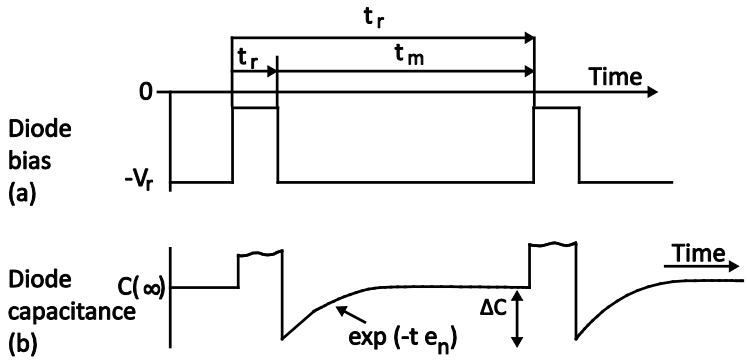

Figure 24 – Diode bias and resulting capacitance including transients from traps are shown. Adapted from Blood and Orton [17].

of 50 ms is assumed sufficient. Then a larger reverse bias is applied creating a depletion region from where the isolated emission process can be studied. Continuing to use the p^+n junction as an example, an increase in the net positive charge density is observed in the depletion region during the emission of trapped electrons. This leads to a contraction of the depletion region and a corresponding increase in the depletion capacitance. After sufficient time, all traps are unoccupied and the capacitance is given by the reverse bias capacitance $C(\infty)$. The development of the capacitance during this cycle can be seen in Figure 24b, and an illustration of the band structure is provided in Figure 25.

By choosing the appropriate values for the reverse bias and the pulse voltages, the depth of the investigated material can be controlled. For example, pulsing with a forward bias reduces the depletion region from the built in voltage, resulting in trapping of carriers in interface defects. On the other hand, the defects in the bulk of the material can be investigated by a zero or small reverse bias during the filling sequence. By obtaining several scans with different bias during the filling sequence it is possible to make a profile of the defect distribution versus depth of the material.

5.4.4 Generating the DLTS signal

The next step is to measure the capacitance transients in a way that reveals the trap properties and makes it possible to separate different trap levels in the system. The concept of the DLTS signal is to weigh the emission rate of the traps against a rate window using a proper weighting function. The rate window is a fixed pre-set value, and a peak is produced in the DLTS signal at the temperature where this value matches that of the emission rate. In its simplest form the DLTS signal can be created from two capacitance measurements separated by a time equal to the rate window; this is known as box-car weighting. The capacitance values are combined by the weighting function, which in this case would be to assign a negative sign to one of the measurements so that the sum becomes the change in capacitance between the two measurements. This is illustrated in Figure 26, where several transients at different temperatures are combined to form the DLTS signal.

The results obtained using a weighting function allows the emission rate to be deduced from the peak position; that is the emission rate value at the temperature corresponding to the peak. In order to map the temperature dependence of the emission rate, several different rate windows are used, placing the

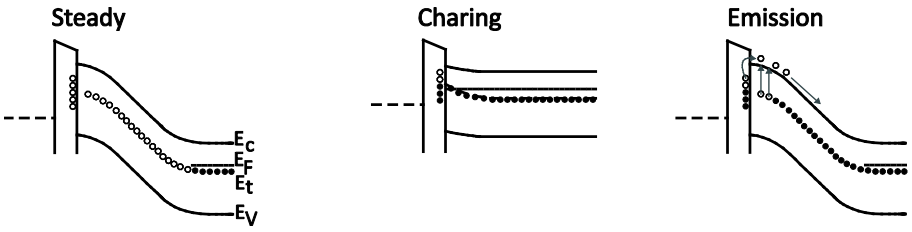

Figure 25 – The steady state of reverse bias is shown to the left. Here all traps in the depletion region are empty. During charging (middle) the traps fill up as the depletion region is removed. Returning to reverse bias the traps empty by the isolated emission process (right). The figure is adapted from [72]

peaks on different temperatures. In this work six different rate windows are used. The signal from the i-th window is defined as

$$S_i(T) = \frac{1}{n_i}\sum_{t_j=t_d}^{t_d+t_i} \Delta C(T, t_j)\omega(t_j) \tag{5.23}$$

where n_i is the number of measurements done in the rate window and t_i is the duration of it. When the depletion region is quenched during the trap filling pulse the capacitance meter might overload, resulting in undesirable values. To recover the instrument from this, a delay time t_d is incorporated between the application of the reverse bias and the first measurement. $\Delta C(T, t)$ is the change in capacitance from the emission from the traps as given by equation (5.22). Finally, $\omega(t)$ is the weighting function.

More sophisticated weighting functions than the simple difference of two measurements mentioned above may be necessary in order to maximize the sensitivity and signal to noise ratio of these measurements. Also the selectivity; that is the ability to distinguish two different peaks, depends on the choice of weighting function. More of the transient is utilized by comparing more than two capacitance measurements. In this work a so called lock-in weighting function is used. It is defined:

$$\omega(t) = \begin{cases} 1 & t_d + 2^{i-1}\tau < t \leq t_d + 2^i\tau \\ -1 & t_d < t \leq t_d + 2^{i-1}\tau \end{cases} \tag{5.24}$$

Using the lock-in weighting function the number of capacitance measurements required is $n_i = 2^i$, τ denotes the time interval between each of the measurements. Thus it can be seen from the definition that the first half of the capacitance measurements are given a negative sign, while the second half is given a positive sign. [73]

With six rate windows and a time interval of $\tau = 10\ ms$, the number of measurements and window lengths is as summarized in Table 3.

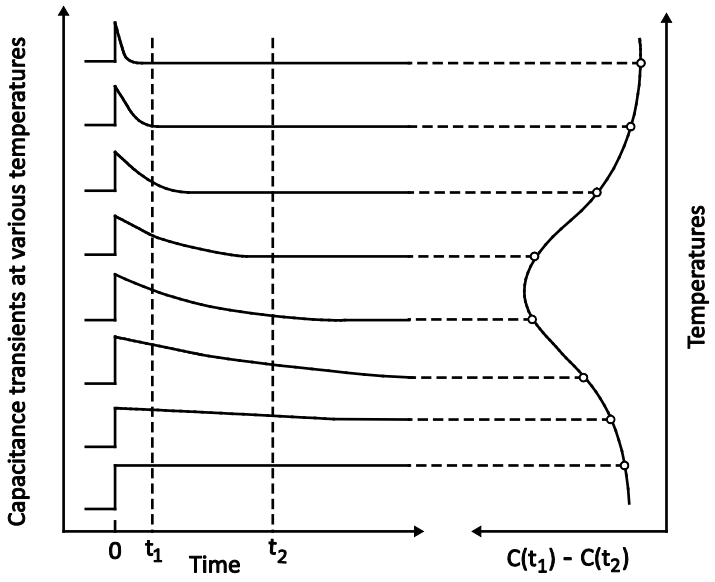

Figure 26 – The capacitance transients to the left is produced at different temperatures. ΔC is largest when the time window, between t_1 and t_2 matches the emission rate. The emission rate's temperature dependence provides a peak on the ΔC versus T plot to the right. By using several different time windows peaks are achieved at different temperatures and the trap signature can be determined. This figure is adapted from Lang [71].

Table 3 – Details for six windows in a lock-in evaluation of capacitance transients.

Window number i	Number of measurements 2^i	Window length t_i $[ms]$	$e_n t_i$	F_i
1	2	20	1.44896	0.12488
2	4	40	1.81717	0.15490
3	8	80	2.09799	0.17597
4	16	160	2.28229	0.18880
5	32	320	2.39056	0.19594
6	64	640	2.44976	0.19971

5.4.5 Data from the DLTS signal

Looking at the DLTS signal in Figure 26, it is clear that the derivative of the signal with respect to the temperature must be zero at the peak. By changing variables this gives the expression

$$\frac{dS(T)}{dT} = \frac{dS}{d(e_n t_i)} \frac{d(e_n t_i)}{dT} = 0 \qquad \textbf{(5.25)}$$

As the last factor is only zero for zero temperature, it is the first factor that is of main interest. With the temperature dependence eliminated the zero-point of the derivative must come from a specific combination of the emission rate and the rate window. For the window length t_i this value of $e_n t_i$ can be calculated numerically by solving equation (5.23) with the lock-in weighting function and values are given in Table 3 for a 5 ms delay time and 20 ms minimum window length. Now the relation between emission rate and temperature can be found by reading out the temperature corresponding to a peak in the DLTS signal from the different windows. The expression for the emission rate in equation (2.22) is repeated:

$$e_n(T) = \sigma_{na}\langle v_n\rangle N_C e^{-\frac{\Delta H}{kT}}, \tag{5.26}$$

and can be rewritten:

$$e_n(T) = \sigma_{na}\beta \mathrm{T}^2 e^{-\frac{\Delta H}{kT}} \tag{5.27}$$

where:

$$\beta T^2 = \nu_{th,n} N_C = \sqrt{\frac{3kT}{m_n^*}} 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{\frac{3}{2}} = \sqrt{\frac{3k}{m_n^*}} 2\left(\frac{2\pi m_n^* k}{h^2}\right)^{\frac{3}{2}} T^2 \tag{5.28}$$

Thus β is a material- and charge carrier property; for electrons and holes in silicon the values are $\beta_n = 3.58{*}10^{21}\ s^{-1}K^{-2}m^{-2}$ and $\beta_p = 1.82\ {*}10^{21}\ s^{-1}K^{-2}m^{-2}$. Rearranging and taking the logarithm of equation (5.27) now yields:

$$\ln\left(\frac{e_n}{T^2}\right) = \ln(\sigma_{na}\beta) - \frac{\Delta H}{kT} \tag{5.29}$$

This equation is used for the derivation of the trap signature. Obtaining the emission rate for several temperatures corresponding to the peaks in different windows allows plotting of $\ln(e_n/T^2)$ versus $1/T$. Such a plot is called an Arrhenius plot, and from this a linear relation is anticipated where the enthalpy of formation of the ionization can be found from the slope and the apparent capture cross section from the intercept with the y-axis.

Also the concentration of traps can be determined from the DLTS signal. Insertion of equation (5.22) into (5.23) yields:

$$S_i(T) = \frac{C(\infty)N_t}{2N_d}\left\{\frac{1}{n_i}\sum_{t_j=t_d}^{t_d+t_i} \mathrm{e}^{-\mathrm{e_n}(T)t}\omega(t_j)\right\} = \Delta C_0 F_i \tag{5.30}$$

Here the expression in brackets is a numerical term F_i that is constant for a given time window; these values are also reported for the parameters used in this work in Table 3. Thus the concentration is given by:

$$N_t = \frac{2N_d S_{i,p}(T_p)}{C_p(\infty)F_i} \tag{5.31}$$

where the subscript p indicates values at the peak temperature.

5.5 ASTERIX EXPERIMENTAL SETUP

The apparatus for IV, CV and DLTS measurements used in this work share a common setup in the lab called the Asterix setup. In this computer controlled environment the data from the different measurements are handled with the LabView software.

The sample holder features a nickel covered alumina plate on where the sample is placed; for good contact with the back side of the sample silver paste is used. The front side is connected with a needle.

Connecting the sample this way allows external rewiring when changing from IV to CV to DLTS, and the measurements can be performed without touching the sample itself. When performing the measurements the sample holder is covered by a metal cap, this is done to protect the sample, avoid illumination and improve temperature control. Cooling is performed with a computer automated lift that lowers the holder into liquid nitrogen. Adjustments are made from response from a temperature sensor located in the sample holder. For IV measurements the data is collected with a Keithley 617 Programmable Electrometer. The capacitance is recorded with a HP4280A for both CV and DLTS measurements, and for the latter the pulsing is provided by a HP8112A.

5.6 SOLAR SIMULATION

The solar simulations were performed with a 91160 Full Spectrum Solar Simulator, from Newport. This provides illumination corresponding to a concentration of 2 suns, and no filter was used, i.e no atmospheric attenuation accounted for. A measurement setup for IV similar to that described in the previous section was used. Parameters for the measurements were chosen in order to observe possible power production in the fourth quadrant, as discussed in section 2.6.2.

5.7 TRANSMISSION MEASUREMENTS

The transmission of light as function of photon energy through a sample can be used to reveal information about the electronic structure. A light source is needed that is able to produce a continuous spectrum of light in the range desired. The light is directed to the sample via a prism. This prism allows scanning of the different wavelengths, and thus energy resolved measurements. Behind the sample is a spherical reflecting chamber where a detector is placed. This way both directly and diffusive transmitted light is detectable.

Measuring thin films gives results also dependent on the substrate, which must be accounted for when deriving the material properties. Using an additional substrate without the thin film, it is possible to do experiments in parallel and utilize the difference. This can also be done in series by calibrating the apparatus with a baseline of the bare substrate. In these methods, the intensity of the light in the two measurements is directly compared by taking the difference. Otherwise, separate measurements of the substrate with thin film and the bare substrate, can be used to approximate the contribution of the film:

$$T_{film} = \frac{T_{film+subst.}}{T_{subst}} \tag{5.32}$$

where T is the transmittance, i.e. the ratio of transmitted to incident light, which is again given by the absorption coefficient $\alpha(E)$ by:

$$T(E) = e^{-\alpha(E)d} \tag{5.33}$$

Here d is the sample thickness and effects such as reflection have been neglected. With a steep onset of absorption the band gap of semiconductors can be deduced directly from the $T(E)$ plots. For amorphous materials the absorption edge is generally not distinct enough for such analysis. An alternative is using the absorption coefficient in so called Tauc plots. These are plots of $(\alpha E)^r$ versus E where different values for r is used. Indirect transitions are described best with $r = 1/2$, while direct band gaps fit better with $r = 2$, either way the band gap can be derived from the intercept with the x-axis. [70]

5.8 HALL MEASUREMENTS

Mobility and concentration of charge carriers can be determined from Hall measurements, as can the resistivity of the sample. The Hall effect describes the transverse electric field that builds up in a conductor that carries an electric current under the influence of a magnetic field. Consider a film of semiconducting material with a magnetic field applied perpendicular to the plane of the film. If a current is conducted across the film in the x-direction the magnetic field will act on the charge carriers with the Lorentz force $F = \pm q\boldsymbol{v} \times \boldsymbol{B}$, where q is the elementary charge, $\boldsymbol{v}$ is the velocity of the charge carriers and $\boldsymbol{B}$ is the magnetic field. The Lorentz force is resulting in acceleration of the charge carriers along the y-axis, perpendicular to the x-axis and the magnetic field. Shifting the charge carriers with a magnetic field this way gives an opposite electric field in the y-direction that eventually cancels the force from the magnetic field:

$$\boldsymbol{F} = \pm q(\boldsymbol{E} + \boldsymbol{v} \times \boldsymbol{B}) = 0 \tag{5.34}$$

This gives $E_y = v_x B_z$. Measuring the direction of the electric field reveals the sign of the charge carriers, i.e. if they are electrons or holes. Considering electrons the velocity is given by the current $v_x = -I/qnA$ where I is the current, n is the electron concentration and A is the cross-sectional area of the semiconductor film. Knowing A and $\boldsymbol{B}$, the electric field can be measured for a controlled current, and from this the concentration of charge carriers can be deduced. The resistivity ρ can be found from Ohms law if the voltage across the sample is measured in the x-direction. Then the mobility can also be calculated from:

$$\frac{1}{\rho} = q(n\mu_n + p\mu_p) \tag{5.35}$$

The use of Ohms law mentioned above requires knowledge of the sample geometry to yield the resistivity, this challenge can be avoided using the van der Pauw method. In a van der Pauw setup four different contact points are defined and alternately used to conduct current and measure the field. From averages of these different measurements the film properties can be extracted regardless geometry of the film. [70]

5.9 X-RAY DIFFRACTION

When studying materials with diffraction techniques, it is the atomic planes of the structure that provide information. The reflected radiation from different planes interferes and provides a diffraction

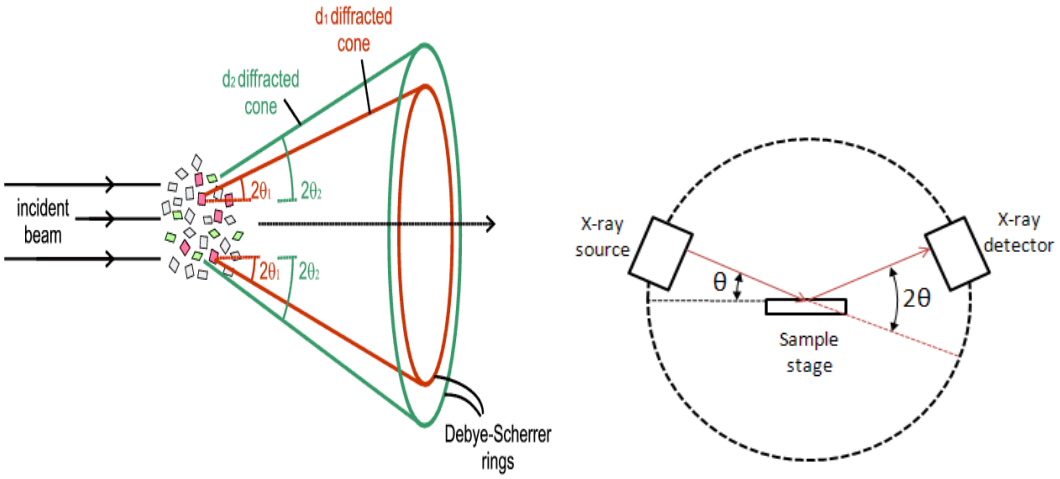

Figure 27 – Diffracted peaks from a powder or multicrystalline material (left). The $\theta - 2\theta$ setup is shown to the right. These figures are reproduced from [74] and [75], respectively.

pattern that is a mapping of the reciprocal structure. Thus the diffraction pattern is a fingerprint for the particular Bravais lattice and the basis in it. To describe planes and directions in the crystal Miller indices are used. A plane is noted $(hk\ell)$ where $h, k,$ and ℓ are reciprocals of the plane's intercepts with the unit cell axis in real space on integer form. In any crystal many planes will be equal due to symmetry; such a family of planes is denoted $\{hk\ell\}$.

For single crystalline materials, the diffraction pattern will be a set of points corresponding to different $(hk\ell)$. Multi-crystalline materials or powders can also be characterized with this technique, then circular diffraction patterns result from diffraction cones as shown in Figure 27, and each circle represent a family of planes $\{hk\ell\}$. Angles and intensities give a unique fingerprint also here. The angles of the cones carry information of the interplanar spacing $d_{hk\ell}$ through Braggs law:

$$\lambda = 2\, d_{hk\ell} \sin\theta \tag{5.36}$$

The intensity of the peaks is given by a structure factor, including information of atom types and coverage in the plane. Identification of materials are done by comparison with material libraries or theoretical data. [8, 76]

$\theta - 2\theta$ scanning is an experimental setup for XRD as shown in Figure 27, the x-ray wavelength is constant so the information on different lattice planes is deduced from varying the angle. The angle is θ between the sample surface and the x-ray source, while the detector moves circularly above the sample with an angle 2θ relative to the transmitted beam. A *Bruker AXS D8 Discover* system has been used for the XRD measurements in this work. Here a copper source provides the x-radiation, and the wavelength used is $k_{\alpha 1} = 1.5406$ Å after removing the $k_{\alpha 2} = 1.5444$ Å with a Göbel mirror.

6 SIMULATIONS

Simulations of the heterojunctions in this work have been done to supplement the experimental work and provide an understanding of the band structure of the device structures. Software from Silvaco was used for the simulations. In the present chapter the first section will introduce the software, a brief review of some previous work is given in the second section, and the third section describes the parameters used in this work.

6.1 SILVACO ATLAS

Silvaco software is a Technology Computer Aided Design (TCAD) tool for semiconductor material technology. Two different branches of the software exist for physically-based simulations of processing and characterization of devices. The simulation of device fabrication can be done with the *Athena* program. This includes models for all the common processes such as lithography, etching, implantation, and diffusion and so on. Simulation of the performance of devices is done with the *Atlas* program, with models for electrical, optical and thermal response to external stimuli. The device input to *Atlas* simulations can be from the *Athena* simulations or, as is done in this work, by defining structural and materials properties on a mesh.

DeckBuild is the tool used to administer the input for the simulation in *Atlas*. Three input categories must be considered for the device simulation: (i) the device structure, (ii) the physical models and (iii) the external biasing. Additionally, a choice of numerical method and output options must be made.

6.1.1 PREPARING SIMULATION

In this work the structure of the device is specified within the input file in DeckBuild. However, it is possible, and convenient for larger structures, to import a structure file. Specifying the structure starts with defining a triangular mesh which is used in the discretization of the structure. A trade-off must be made between accuracy and numerical efficiency when choosing the density of the mesh. To increase efficiency the mesh can be finer in regions with rapid changes in properties such as at interfaces, and coarser in the bulk material. A gradual change in the density is recommended to avoid problems with continuity convergence in the calculations.

When the mesh is defined, the next step is to specify regions of different materials. Databases of material properties exist with varying degree of detail and it is also possible to change any parameter of choice. Doping and defect concentrations are also specified in this section. Finally, electrodes must be defined on the device surfaces.

Selection of physical models is the next step. A range of models for mobility, carrier concentration, band gap narrowing, recombination and other properties are available, and an appropriate choice must be made for the results to be accurate. A selection must also be made from available output

parameters. Finally a suitable numerical method must be chosen to do the calculations. For reference an input file used in this work is provided in Appendix 9.1.2.

6.2 PREVIOUS MODELING WORK

In a previous master thesis by Tang [77] simulation results for traps in a Schottky contact with Pd on ZnO were fitted to experimental data. The trap model was then brought along into simulations of ZnO/Si heterojunctions with both n- and p-type Si. Simulations of the heterojunctions were done varying the electron affinity of ZnO χ_{ZnO} between 3 and 5 eV as this was the span of experimental values from literature at the time. For simulations with n-type Si high rectification and photovoltaic efficiency was found using the higher values for χ_{ZnO} and high concentration of interface electron traps. P-type substrates on the other hand exhibited lowered photovoltaic efficiency with increasing acceptor trap concentration. Literature review shows more examples and higher efficiency in samples with n-type Si than p-type. Thus it was concluded that the electron affinity for ZnO is higher than for Si and that electron traps are present on the interface. As mentioned in section 2.8 the work function of ZnO hs recently been determined at $\phi_{ZnO} = 4.65 \pm 0.1\ eV$ [51], which is , indeed, higher than that for n-type Si.

6.3 SELECTING SIMULATION PARAMETERS

Both the n-type and p-type wafers used experimentally in this work have doping concentration close to $10^{15}\ cm^{-3}$. Comparing to the degenerate ZnO films with carrier concentration on the order of magnitude $10^{20}\ cm^{-3}$ it is clear that the approximation of an asymmetrical junction holds. Using equation (2.27) it can be seen that the extent of the depletion region is less than 4 μm for the relevant biasing. For the simulations a finer mesh is used in the depletion region than for the neutral region in the rest of the wafer thickness. Close to the junction and the thin buffer layer an even finer mesh is needed.

A library of material properties is available through the software. For high quality crystalline silicon wafers, it is little reason to doubt the validity of such data based on the extensive knowledge that exist for this material. ZnO properties are also available in the database, but building on less available values from literature, larger uncertainties are associated with these values. ZnO database values are however assumed sufficiently accurate for this work except the electron affinity which is altered to 4.65 eV. For the amorphous buffers crystalline data for Si, SiGe and SiC(6H) are the basis. The *Atlas* user's manual [78] suggests adaptions to the Si data to simulate aSi. These are followed, and analogous adaptions are performed for the other materials, as summarized in Table 4. The suggested band gap for aSi is in the high end of achievable values according to literature, but found appropriate comparing to the expected band gap from the PECVD deposited films in this work. For aSiGe the band gap can be varied between 1.0 and 1.7 eV depending on the germanium concentration [79]. A large span in band gaps is available also for aSiC depending on the polytype, and values ranging from 1.5 to 3.0 eV have been reported [58, 59]. With a relatively small fraction of Ge in the experimental

samples, the most extreme deviations from the pure Si values cannot be expected. Some variation is however expected so a value of 1.4 eV is chosen for modelling of aSiGe. For aSiC a band gap of 2.4 eV is assumed. The values used are summarized in Table 4. The low field hole mobility μ_p has been reported to not vary significantly with alloying with either Ge or C, while a decrease is found for the low field electron mobility μ_n for both [80]. An order of magnitude reduction is assumed in this simulation. For the crystalline silicon and ZnO models for field-dependent mobility are used, the resulting values are at least an order of magnitude larger than the mentioned values for aSi. Along with these models several models for carrier concentrations and recombination properties are used, some explanatory comments can be seen in the input file in appendix 9.1.2. Further details are available in [78], and will not be discussed here. In a review by Ellmer et al. [81] an effective mass $m^* = 0.5m_0$ is reported for ZnO with electron concentrations exceeding $10^{20}\ cm^{-3}$ due to non-parabolicity of the band structure. This is further expanded in [38], and gives an effective density of states in the conduction band close to $9 * 10^{18}\ cm^{-3}$.

The heterostructures have been treated with the affinity rule to divide the difference in band gap. Transport across the interfaces is modeled with thermionic emission and tunneling.

Table 4 – Material properties used in the simulations in this work. The simulations were performed with values for $T = 300\ K$.

	ZnO	Si	aSi	aSiGe	aSiC
ϵ	8.49	11.8			
$E_g\ (eV)$	3.37	1.12	1.9	1.4	2.4
$\chi\ (eV)$	4.65	4.05	3.93 [82]		4.12 [83]
$N_C\ (cm^{-3})$	$9 * 10^{18}$	$2.8 * 10^{19}$	$2.5 * 10^{20}$	$2.5 * 10^{20}$	$2.5 * 10^{20}$
$N_V\ (cm^{-3})$	$1.8 * 10^{19}$	$1.04 * 10^{19}$	$2.5 * 10^{20}$	$2.5 * 10^{20}$	$2.5 * 10^{20}$
$n_i\ (cm^{-3})$	$3.11 * 10^{-10}$	$1.45 * 10^{10}$			
$\mu_n\ (cm^2/Vs)$			20	2	2
$\mu_p\ (cm^2/Vs)$			1.5	1.5	1.5

PART III: RESULTS AND DISCUSSION

7 RESULTS AND DISCUSSION

In this chapter the experimental results are presented and discussed. First, the simulation results are presented in section 7.1. Then characteristics of the deposited films are assessed through the results from transmission, Hall and XRD measurements in the next section. Results from measurements of current (IV) and capacitance (CV) are presented in section 7.3, and then the temperature dependences of these are reported in section 7.4. Characterizations of the interface defects through DLTS are reported in section 7.6, and finally, in section 7.7 the photovoltaic response of the samples is presented.

7.1 RESULTS FROM SIMULATIONS

In this section the band diagrams obtained from the simulations are shown, followed by the corresponding IV curves. Figure 28 shows the band diagrams for the structures on both n-type and p-type, without buffer layer. Throughout the figures of the band diagrams, the ZnO film is to the left, and the silicon wafer extends to the right. The full wafer thickness is not shown, in order to focus on the band bending and buffer layer in the junction. The conduction band edge is given in red, the valence band edge in blue and the green line is the Fermi level. Barrier heights can be read out from the band diagrams, and the values obtained are $\phi_{bn} = 0.53\ eV$ and $\phi_{bp} = 0.58\ eV$ on n-type and p-type, respectively, when using electron concentration $N_d = 1 * 10^{20} cm^{-3}$ for the ZnO, as here.

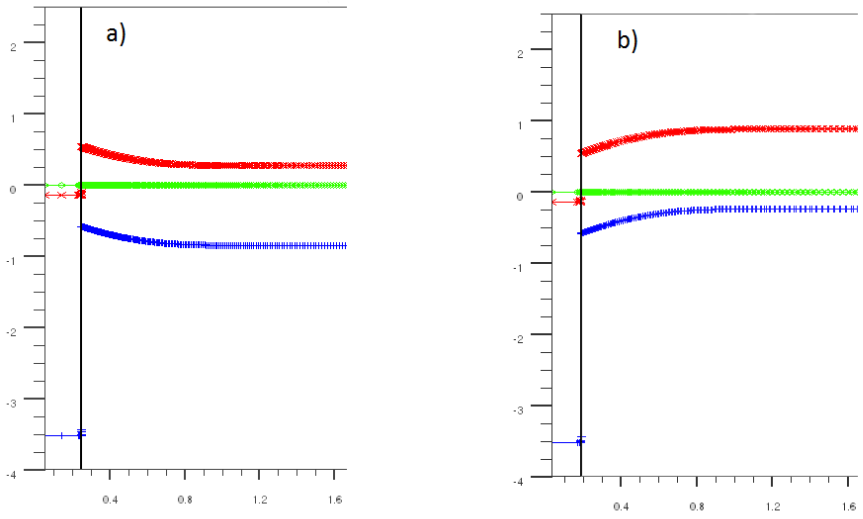

Figure 28 – Simulated band structure for the ZnO/n-Si heterostructure (a) and ZnO/p-Si (b).

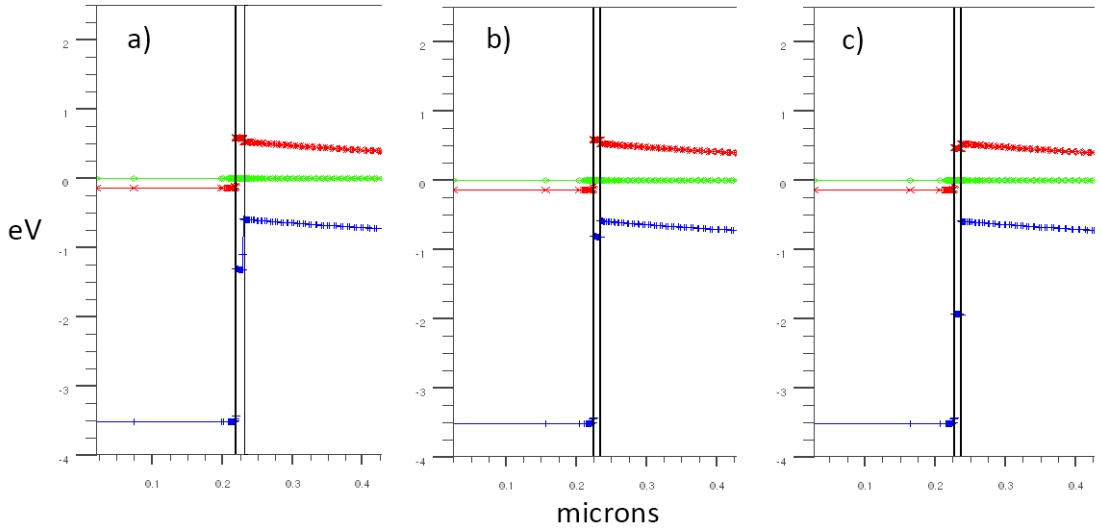

Figure 29 –Simulated band diagrams for the structures ZnO/buffer/Si with n-type Si substrates. 10 *nm* buffer layers are used, with compositions aSi (a), aSiGe (b), and aSiC (c).

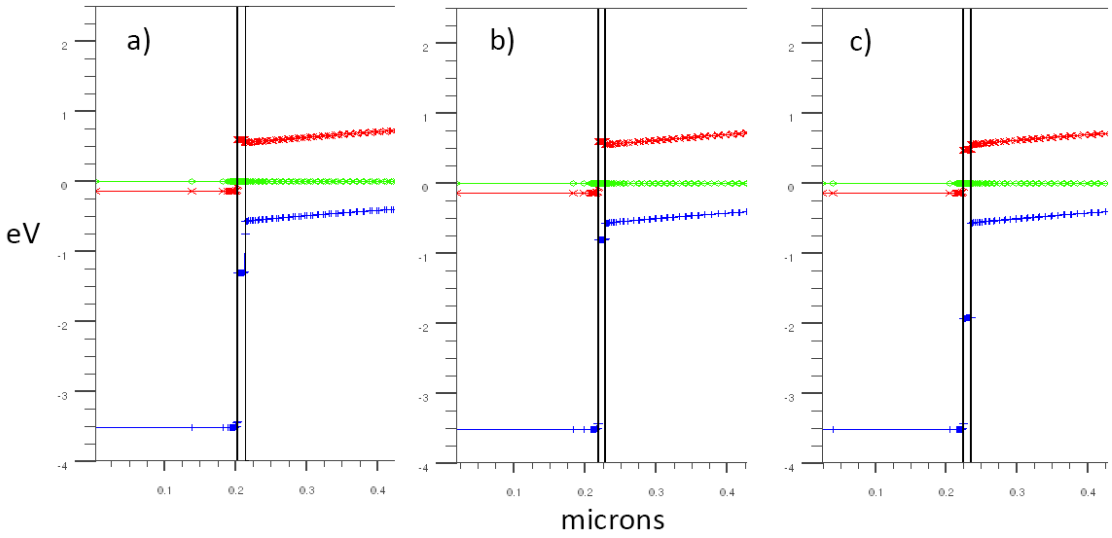

Figure 30 – Simulated band diagrams for the structures ZnO/buffer/Si with p-type Si substrates. 10 *nm* buffer layers are used, with compositions aSi (a), aSiGe (b), and aSiC (c).

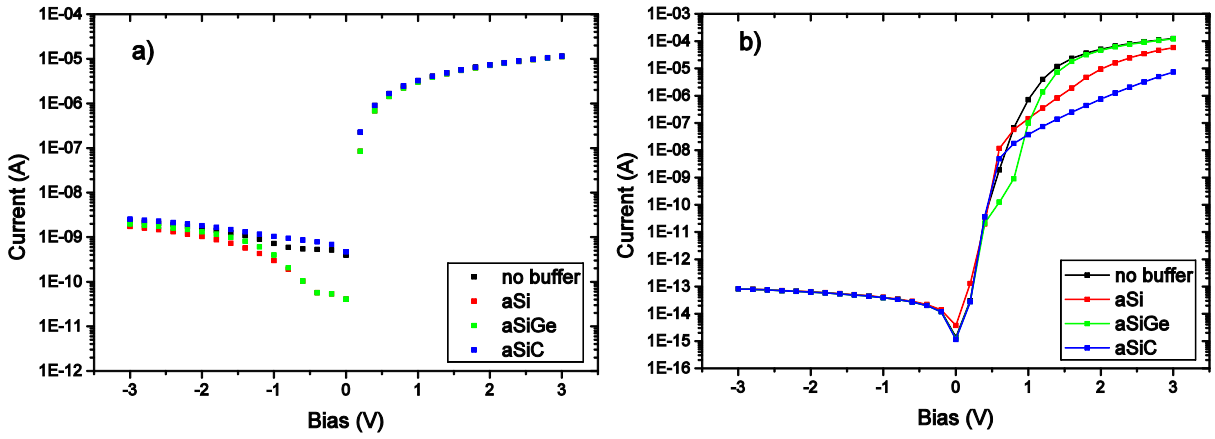

Figure 31 – For the n-type (a) and p-type (b) substrates, simulation results for the IV characteristics of the different sample structures studied. Notice the different y-scales of the two panels.

For structures on n-type substrate with buffer layers, the band diagrams are depicted in Figure 29, and the similar structures on p-type substrates are displayed in Figure 30. As the work functions that have been used in the simulations are similar, the largest influence of the different band gaps is seen in the valence band of the structures. Thus it may be expected that the buffer layers provides a stronger influence on the samples with p-type substrates. This is reflected in the simulated IV curves presented in Figure 31, where the forward current in structures with p-type substrate (a) depends on the buffer type, while the current in n-type structures (b) do not.

7.2 CHARACTERISTICS OF DEPOSITED FILMS

7.2.1 ZINC OXIDE

The ZnO film deposited on glass substrate was used to characterize the resistivity and carrier concentration through Hall measurements. From the same sample, the band gap was estimated from the measured transmission spectrum.

The Hall measurements were carried out at room temperature with a van der Pauw setup using magnetic fields of ± 5 and $10\ kG$. From these measurements resistivity $1.57 * 10^{-3}\ \Omega\ cm$ and carrier concentration of $5.96 * 10^{20}\ cm^{-3}$ are obtained.

The transmission spectrum was recorded in a wide range from 2600 to $290\ nm$, as shown in Figure 32. The step observed at $800\ nm$ is due to the transition between two different sensors, and it is believed that the low wavelength range yields the more accurate values. The high wavelength range is included as a qualitative visualization of the plasmon damping as briefly mentioned in section 2.8.1. The inset shows the $300 - 800\ nm$ range. The wave pattern is an interference artifact resulting from the thin film. Taking the mean of this oscillation to represent the real transmission value, yields the value $83\ \%$ in the $400 - 800\ nm$ range. A linear fit has been performed on the steep descent of the

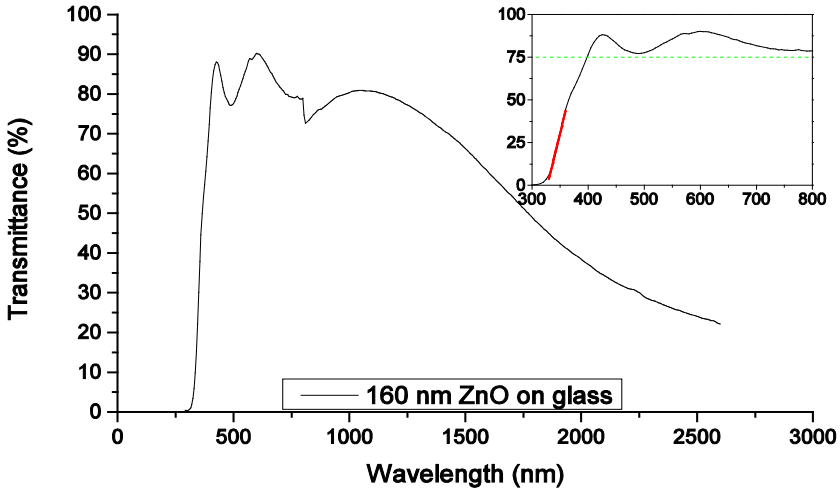

Figure 32 – Transmission spectrum from the ZnO sample on glass substrate. The inset is an enlargement of the visible region.

curve as this relates to the initiation of absorption across the band gap. The resulting intercept with the abscissa is at $327\ nm$ indicating an optical band gap of $3.79\ eV$.

This indicates a significant blue-shift, described as the Burstein-Moss effect from the Fermi level being moved into the conduction band. The magnitude seen here is greater than indicated in the discussion in section 2.8.1, but in agreement with values reported in [37].

7.2.2 BUFFER LAYERS

The thicknesses of the buffer layers used in the HIT structure are too thin for reliable measurements with XRD, Hall and transmission. Thicker depositions of the buffer materials with germanium and carbon were therefore performed on glass substrates for isolated evaluation of electronic, structural and optical properties. The thickness of these films was approximately $50\ nm$. In addition to the as-deposited samples, annealing was also carried out both in nitrogen ambient, to simulate the heating for buffers during ZnO deposition, and in forming gas. For all measurements a high resistance was found, precluding the use of Hall measurements, and indicating intrinsic films with low carrier concentrations. In transmission measurements little difference was seen from the thin film samples compared to the reference of an untreated glass substrate, rendering the determination of a band gap value difficult.

Slightly more absorption was seen in the samples exposed to nitrogen during annealing compared to the others. Further investigation of the optical properties of these was performed by Dr. Augustinas Galeckas by repeating the transmission measurement and performing photoluminescence (PL) measurements. From transmission data, the influence of the deposited thin film was separated from the glass substrate by calculating the ratio of transmission from the sample with thin film to the bare reference substrate. The absorption coefficient was deduced from these data and plotted as Tauc plots

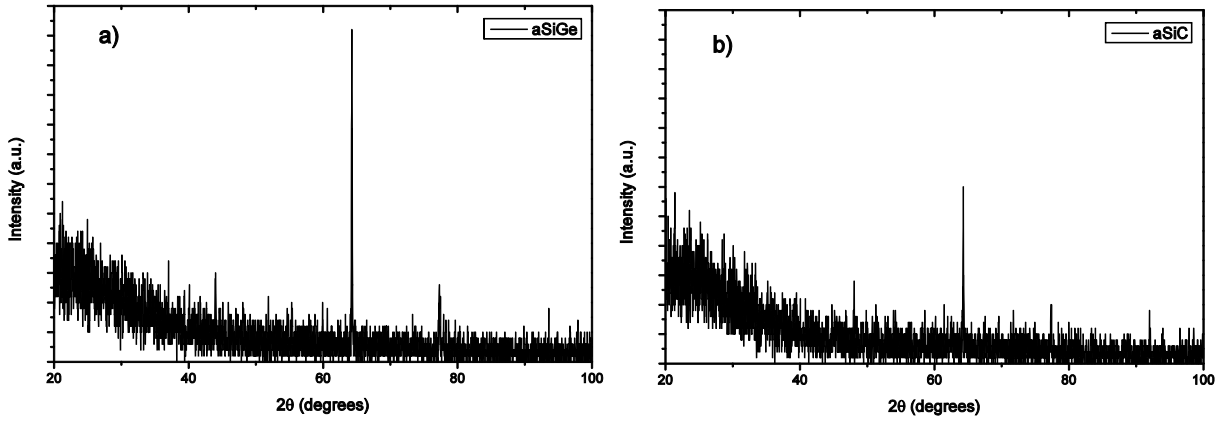

Figure 33 – X-ray diffractograms of the ~50 nm films of aSiGe and aSiC on glass substrate. The graphs shown are from samples annealed in a nitrogen gas flow at 400 ℃.

as described in section 5.7 for $r = 1/2$ and 2. None of the samples show clearly defined linearity for either r-value. For the plots adapted to indirect band gaps it can however be argued that some linearity in several regions exists. These indicate energy spans $1.5 - 3.3\ eV$ and $1.7 - 3.3\ eV$ for samples with aSiGe and aSiC layers, respectively.

Photoluminescence (PL) is the emission of light from a material in response to exposure to a high energy light source that excites charge carriers over the band gap. This emission comes from the direct, radiative recombination of charge carriers. Studying the emission as function of energy can thus provide information on the electronic structure. The penetration of the incident light into the material depends on the absorption coefficient. Higher energy UV light reduces the absorption length and confines the investigated volume to the surface. A $4\ eV$ source was used here. However the thickness of $50\ nm$ is still thin and contribution from the glass substrate is strong. Additionally a glass substrate is far from ideal due to relatively high activity in a broad energy range. As for transmission these measurements were done on both the deposited films and on the bare glass substrate. The difference between the two was determined in an attempt to isolate the contribution from the thin films. A gradual onset of emission with higher energies and broad peaks are the result. This indicates again that there is no clearly defined band gap. For both aSiGe and aSiC a broad peak at close to $3\ eV$ is present, in addition to a peak at approximately $1.8\ eV$ with much lower intensity. The aSiC material additionally shows an intermediate shoulder at $2.4\ eV$, the latter possibly indicative of cubic SiC inclusions.

XRD was also performed on these samples. Figure 33 shows the result from the samples annealed in a nitrogen gas flow at 400 ℃. The line seen just above 60° has fairly low intensity and is attributed to the glass substrate as it shows up also in measurements of the untreated substrate. Also the *As-Deposited* samples, and those annealed in forming gas flow, yield similar diffractograms. This indicates that the sputter deposition yields amorphous films, and that the 400 ℃ annealing associated with the ZnO deposition does not initiate crystallization of the films. For several reasons this is, however, not conclusive proof that the buffer layers in the heterostructure are amorphous. Firstly, the buffer layers are significantly thinner than the depositions on the glass substrates. Secondly, the Si substrates provide different chemical and structural basis for the sputtered films. Lastly, the deposition

of AZO on top of the amorphous films may also contribute as a driving force for crystallization. For example by Metal-Induced Crystallization (MIC), which can be utilized as a technique to produce polycrystalline Si films at low temperatures, starting from films of amorphous Si and a suitable metal, typically Al [84]. Breivik et al. [85] have suggested such crystallization in the AZO/aSi/Si heterostructure as well as for the similar structure with undoped ZnO.

7.3 CURRENT AND CAPACITANCE MEASUREMENTS

Room temperature IV and CV measurements were performed for all samples, and for each sample several diodes were measured. For each diode, the IV and CV measurements were carried out without moving the probe that connects the diode to the measurement apparatus. The rewiring is done externally on the sample holder. Several diodes on each sample were measured, and also reproduced by removing and reapplying the silver paste backside contact. Some variations were seen with different diodes on the same sample, as will be discussed later. Presentation of the averages of these measurements may be considered as a means of giving a fair illustration of the samples performance. This idea was however rejected, as deviations on some diodes lead to loss of details, particularly in the current under reverse bias. Instead the best diode have been chosen for the presentation of the results here, although the variations have been kept in mind. The discussion of homogeneity in the deposited films in the next section is partly motivated by this variation. The best diode was also used for the temperature dependent IV and CV measurements as well as the DLTS. The notion of a "best" diode leaves room for interpretation; here the IV measurements were used for evaluation and high rectification and a small ideality factor were determining factors. It must be emphasized that for most samples several diodes show properties close to the best ones, and the large variations were often related to poor backside contacts thus not an indicator of the sample quality.

The IV data are plotted on a semi-logarithmic scale as described in section 5.1.1. Ideality factors have been evaluated for the longest possible linear region at low forward biases. Where rectification is mentioned, it is referring to the difference in current between forward and reverse bias; at $\pm\ 3\ V$. For the CV measurements plots of $1/C^2$ as function of V are essential to the evaluation of the sample properties, as has been discussed in section 5.2. These are co-plotted with $C(V)$ in the following data presentation. The $1/C^2$ plots show good linearity for most samples, with some slight exceptions for the lowest biases. Ignoring these, the doping levels of the silicon substrates deduced from the linearity correspond well to the wafer specifications. For the n-type samples values in the range $9.2 * 10^{14}$ to $1.15 * 10^{15}\ cm^{-3}$ are found, and the p-type samples gives values from $8.0 * 10^{14}$ to $9.8 * 10^{14}\ cm^{-3}$.

7.3.1 SAMPLES WITH PECVD aSi BUFFER LAYERS

Figure 34 and Figure 35 show the IV and CV data obtained from measurements of the samples with buffers deposited with the PECVD technique. Results from the samples prepared without buffer layers are also displayed in these figures, as they were produced with the same deposition of AZO. For increased readability, the n-type samples are kept to the left and p-type to the right throughout the chapter. With an overall look it is interesting to note that rectification of at least five orders of

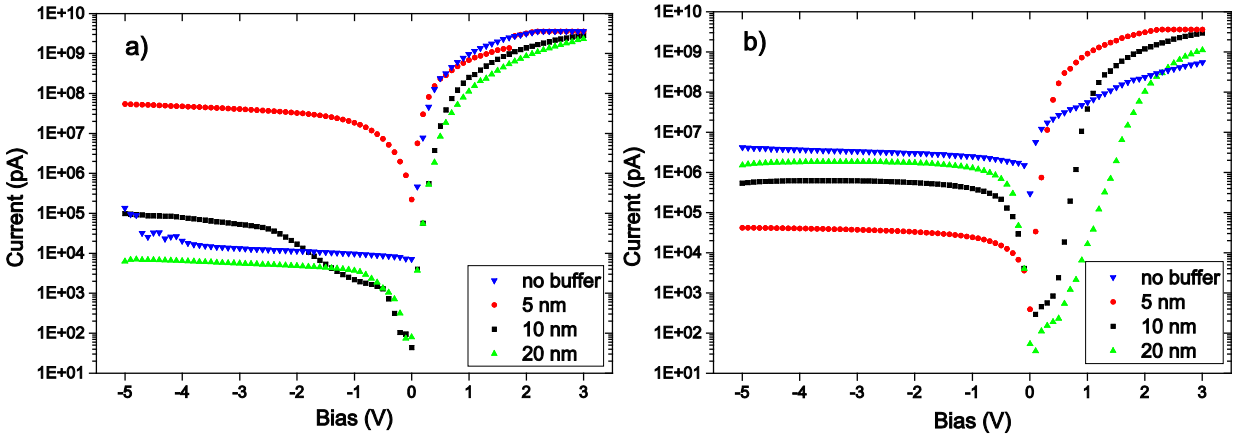

Figure 34 – IV characteristics for the first batch of samples, with buffer layers of aSi deposited by PECVD. Samples with n-type substrates are shown to the left (a) and with p-type substrates to the right (b).

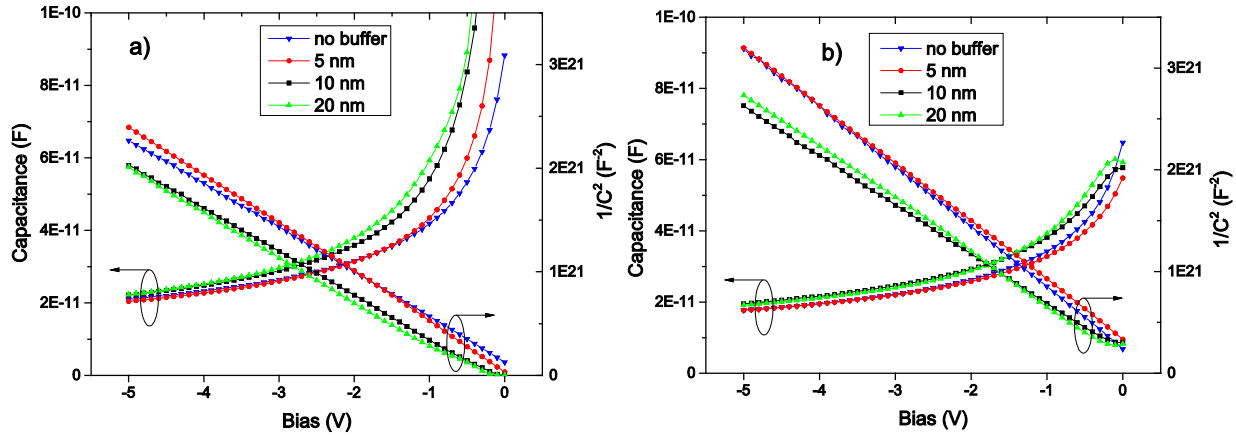

Figure 35 – Capacitance data of PECVD samples on n-type (a) and p-type (b) substrates. The curved graphs are plots of C(V) with y-axis to the left, while plots of $1/C^2$ vs V are close to linear with values on the right side y-axis.

magnitude is possible on both substrates. Comparison of the similar samples on n-type and p-type substrates can hint of the quality of the junctions. According to the Schottky-Mott model the sum of the two barrier heights should equal the silicon band gap. Agreement to this model is found for ZnO grown by Atomic Layer Deposition (ALD) on Si reported by Quemener et al.'s [51]. For the samples without buffer layers in the present work, such an agreement is less evident. Here, the barrier height for the samples without buffer sum to 1.39 eV when deriving their values from the linear part of the forward bias in the IV measurement, and 1.29 eV when considering CV data. The high values and the difference between methods indicate deviation from the Schottky-Mott model, as will be discussed later. All values deduced from the measurement results is summarized and compared in section 7.3.6.

Besides the preceding notion, the comparison of n- and p-type samples is perhaps of secondary importance. This is because they rely on different charge carriers and parts of the electronic band structure. More important is comparison of different samples on the same substrate and trends from these results.

SAMPLES ON N-TYPE SUBSTRATES

The IV characteristics of the structures deposited on n-type substrates are shown in Figure 34a .The most striking feature of the IV curves of the n-type samples is the 5 nm sample with its high reverse current compared to that of the others. All diodes on this sample show similar features, also after removal and re-application of the silver paste backside contact, indicating that the features are not influenced by the backside Ohmic contact. Deposition of aSi and ZnO on this sample were done simultaneously with the corresponding p-type sample showing no such irregularity. Still, some contamination of the sample cannot be ruled out.

For the sample without buffer and with 5 nm buffer the steep increase in current during forward bias indicate non-linearity with the uneven spacing of the measurement points. A linear fit is still used to deduce ideality factors and barrier heights. Using these values, and fitting with the analytical series resistance model from section 5.1.2 gives good agreement to the measured data. Hence, the values for ideality factor and barrier height are considered reliable. The values achieved for ideality factors are 1.11 and 1.99 for no buffer and 5 nm buffer, respectively. The high value obtained for the 5 nm sample indicates significant recombination in the depletion region. Combined with the high current under reverse bias it is considered a sign of poor interface quality and this issue is further pursued with the DLTS measurements presented in section 7.6.2. For the samples with 10 and 20 nm buffers good linearity is seen, and their ideality factors are found to be 1.25 and 1.33. The barrier heights deduced from these two are similar, but higher than that of the sample without buffer. No clear trend in the response to buffer thickness can be deduced from these IV plots when it comes to ideality factor or barrier height. Series resistance on the other hand is found to increase with thicker buffer layers. For the sample without buffer a value of 600 Ω is obtained, and an increase to 1 $k\Omega$ is observed for the sample with 20 nm buffer. For the sample without buffer, saturation of the curve is seen above 2 V forward bias. This is in addition to the series resistance, and attributed to the range limitation for the measurement apparatus.

Upon evaluating the linear region of the IV measurements, the reverse saturation current is calculated from the intercept with the y-axis at zero voltage. This value is found to differ from the reverse current observed at reverse biases and a discussion follows in section 7.3.6. The exception is the sample without buffer, at least if the increase in current below $V = -4\ V$ is neglected. Using the values deduced from the linear region on this sample gives a good fit with the diode equation (2.29) also under reverse bias.

The CV plots, in Figure 35a, show increasing capacitance for increasing buffer thicknesses. Intersection of the $1/C^2$ lines with negative x-axis values precludes evaluation of the built-in voltage in the two samples with the thickest buffers. Such negative values are non-physical, but may sometimes be associated with a high conductance. However, no significant deviation in the conductance is observed in the output from CV measurements. Another possible explanation relates to the presence of the buffer layer, and the development of the depletion layer as a function of applied voltage. No significant deviation is seen in the slope of these samples compared to the sample without buffer, and the capacitance is higher for all biases. As the capacitance is proportional to the reciprocal of the depletion thickness this may point at an underdeveloped depletion region compared to the

theoretical model. This can come from voltage loss or parasitic capacitance on the sample away from the junction.

SAMPLES ON P-TYPE SUBSTRATES

For p-type substrates, in Figure 34b, the sample without buffer shows rectification of only two orders of magnitude. Even though this is low compared to other samples in this batch it is not too far from the expected results looking at the dependence of deposition temperature investigated by Quemener et al. [48]. A large series resistance of almost $5\ k\Omega$ is associated with this sample. These results are also in good agreement with results reported by Chaabouni et al. [86] for their sample sputtered at 400 ℃.

For the samples with buffer layers there is a clear trend; significant reduction in the observed reverse current and thus increase in rectification is observed with reduced buffer thickness. An equally significant decrease is seen in the ideality factor. Going from thick to thin buffer the ideality factors are 4.15, 1.85 and 1.14 and the corresponding values for the barrier height are 0.95, 1.03 and $0.80\ eV$. For these samples fitting with the analytical solution with series resistance gives good coherence in the forward region, and values obtained are $600\ \Omega$ for the 5 and $10\ nm$ sample and $750\ \Omega$ for the $20\ nm$ sample. These trends were contributing to the choice of buffer thicknesses chosen for the sputtered samples discussed in the next subsection.

The CV measurements, in Figure 35b, for the p-type samples all give positive values for the built-in voltage. The magnitudes, however, vary quite drastically, and the resulting barrier heights are between $0.56\ eV$ for the $20\ nm$ sample and $0.86\ eV$ for the $5\ nm$ sample.

7.3.2 SAMPLES WITH SPUTTERED aSi BUFFER LAYERS

The samples with sputtered aSi are reported and discussed in this subsection. Figure 36 and Figure 37 show IV and CV curves for the two different buffer thicknesses, including the additional $5\ nm$ samples where also the ZnO deposition was done at room temperature.

SAMPLES ON N-TYPE SUBSTRATES

For the n-type samples a large difference is seen in the two different $5\ nm$ samples in Figure 36a. The room temperature deposition sample shows significantly higher current, especially under reverse bias, thus lowering the rectification. A possible explanation is that the low temperature deposition of ZnO results in a poorer quality film, with more defects and residual stress. It may also indicate that annealing of interface states occur during the ZnO deposition at 400 ℃. The same difference is not seen in the p-type samples, and from this difference it can be suggested that the defects are more active with respect to electrons than holes. These explanations will be reviewed when looking at the DLTS spectra of the samples.

As observed for the PECVD samples, the capacitance is higher for the thicker buffer of the two samples deposited at 400 ℃. Further, an even higher capacitance is observed in the room temperature deposited sample, which can again come from voltage drop or parasitic capacitance as discussed in the previous subsection. Corresponding to the high reverse current in the IV measurements, this can possibly be attributed to a high concentration of interface defects.

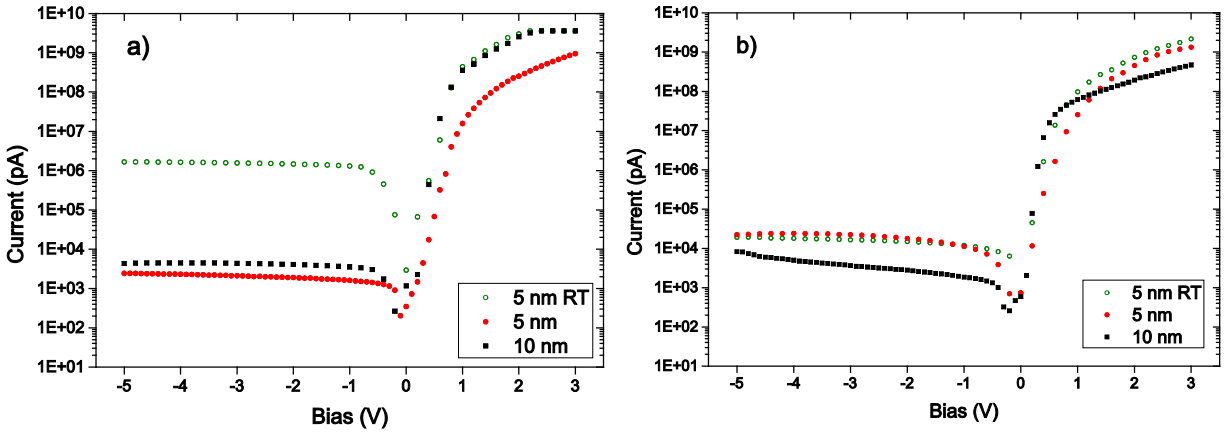

Figure 36 –Samples are with aSi buffers of 5 and 10 nm thickness on n-type (a) and p-type (b). Two different versions of the 5 nm samples are included. One is with the whole sputtering deposition, including AZO, performed at room temperature (RT). The other is with AZO deposited at 400 ℃, as is the case for the 10 nm sample and all remaining samples.

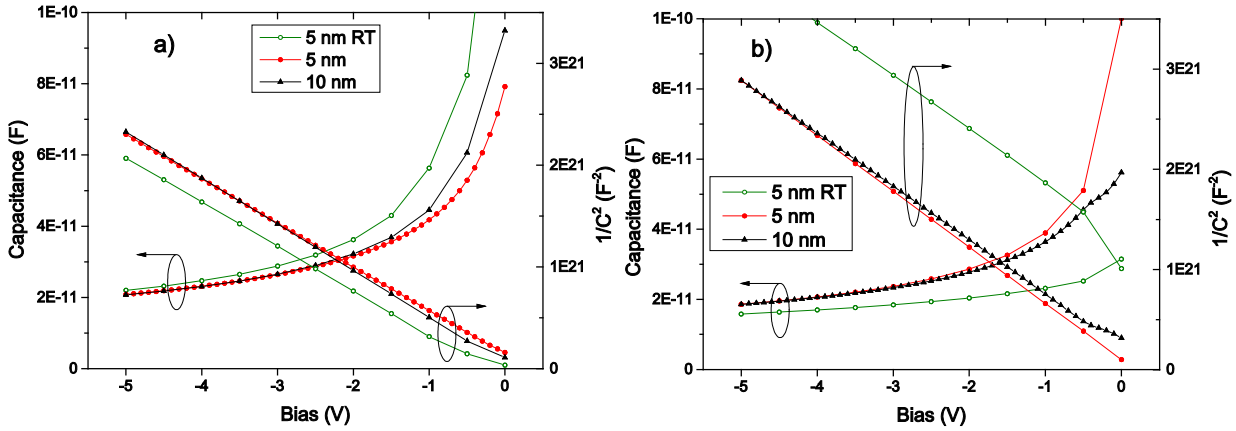

Figure 37 – CV measurements of the samples with sputtered aSi buffer on n-type (a) and p-type (b).

Ideality factors on these samples are poorer than their PECVD equivalents, as expected due to the performance of the deposition technique used. The room temperature deposition gives a value of 3.08, and a slight improvement is seen to the 400 ℃ deposition with a value of 2.92. The 10 nm sample is better with a value of 1.69. These high values imply that the thermionic emission model is insufficient in the description of the current transport mechanism.

Samples on p-type substrates

The two 5 nm samples on p-type substrates behave almost identically with respect to IV characteristics with barrier heights calculated to be 0.78 and 0.79 eV for the RT and 400 ℃ sample respectively. This is also in good agreement with the value seen in the corresponding PECVD sample. The RT sample has a better ideality factor at 2.34 compared to 2.65 for the 400 ℃ deposition. The 10 nm sample has approximately the same rectification, but with lower current in the whole bias range. Its steeper forward bias characteristics give an ideality factor of 1.21 and a barrier height of 0.84 eV.

With the similar behavior of the 5 nm samples in the IV measurements, the large deviation in CV is unexpected. The low capacitance values of the RT sample give a high $1/C^2$ plot, and correspondingly

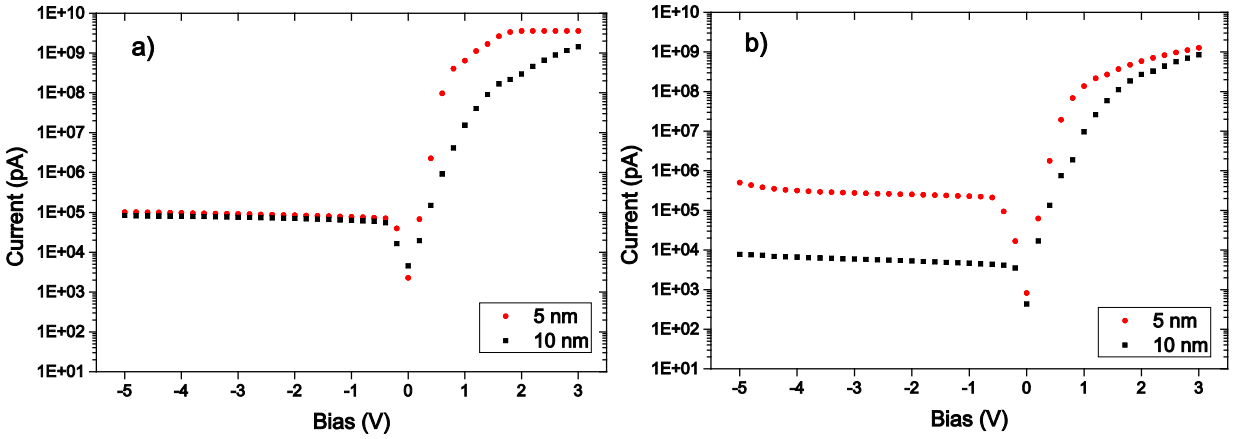

Figure 38 – IV curves for samples on n-type (a) and p-type (b) substrates with aSiGe buffer.

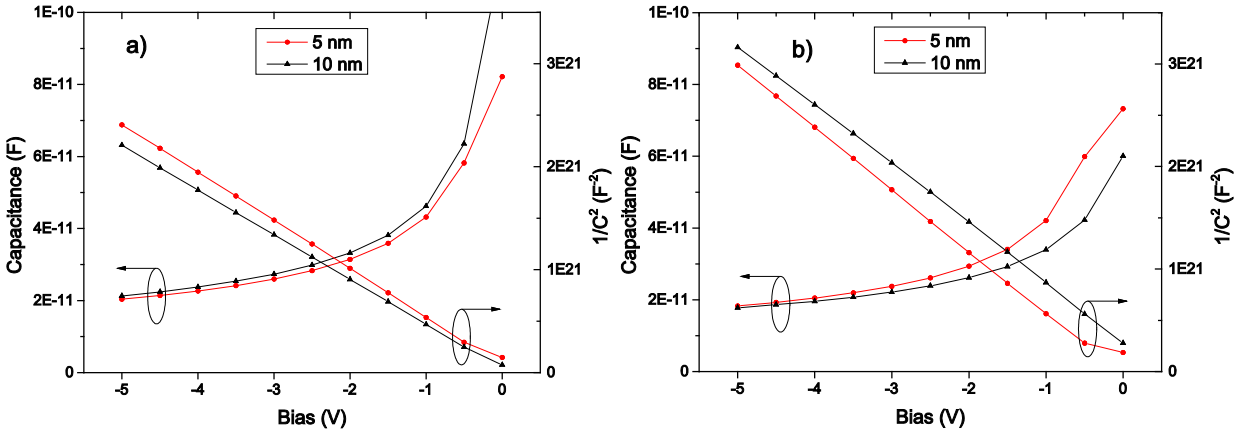

Figure 39 – CV measurements of the same samples presented in Figure 38.

high implied built-in voltage at 2.42 *eV* which is 2 *eV* higher than that of the 400 °C deposition. The value of 0.70 *eV* found for the 10 *nm* sample is, on the other hand, more as expected.

7.3.3 SAMPLES WITH SPUTTERED aSiGe BUFFER LAYERS

Figure 38 and Figure 39 show the measurement data from the samples with aSiGe buffers.

SAMPLES ON N-TYPE SUBSTRATES

As above, the ideality factors deduced from the IV measurements are relatively high, and the obtained values are just above 2 for the 5 *nm* and above 4 for the 10 *nm* on n-type. Hence, the junction characteristics deviate from the thermionic emission model.

Comparing the IV measurements to the samples with aSi buffers deposited under the same conditions it can be seen that the aSiGe samples exhibit a higher current at reverse bias. This suggests a lower barrier in the aSiGe samples, in accordance with the lower band gap of aSiGe, but questioning the choice in electron affinity made for the simulation of this structure. A similar trend is seen in values for reverse saturation current obtained from the linear region during forward bias. The derived barrier heights are 0.80 and 0.78 *eV* for the 5 and 10 *nm* sample, respectively, which is about 0.1 *eV* lower than the corresponding samples with aSi.

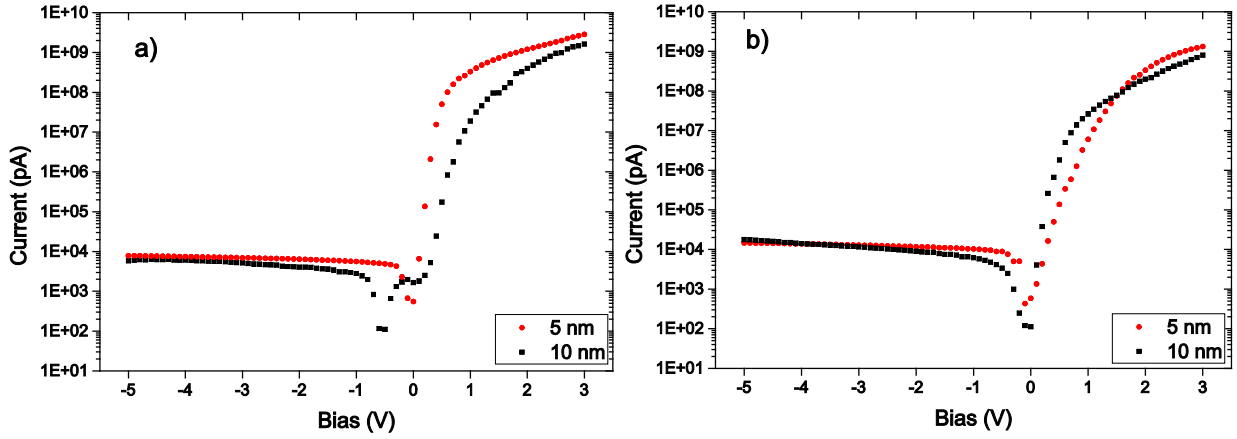

Figure 40 – aSiC buffer layers of thickness 5 and 10 nm are shown in this figure, on n-type (a) and p-type (b) substrates.

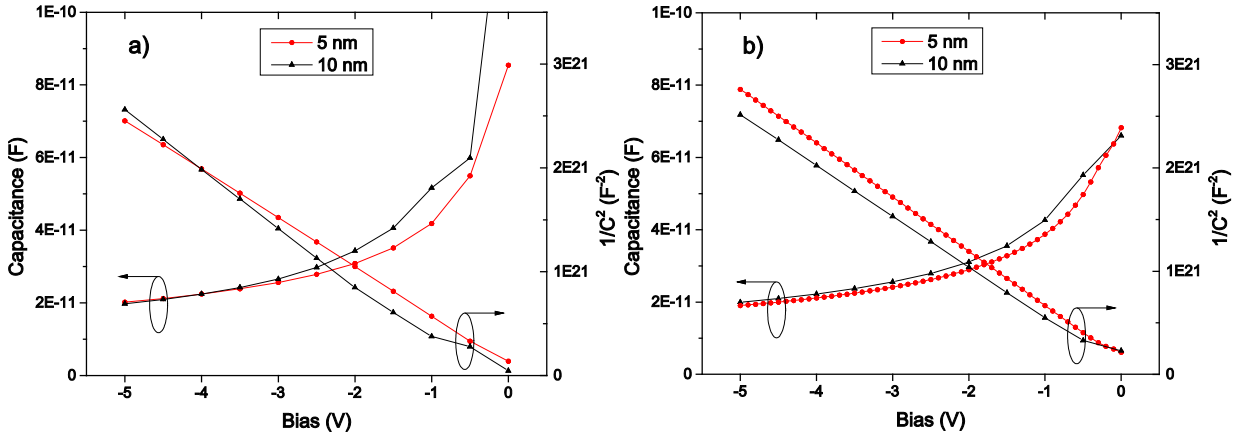

Figure 41 – CV data corresponding to the IV plots in the above figure.

The CV data again follow the trend of higher capacitance for the thicker buffer on n-type substrates, while low values for the built-in voltage also result in low barrier heights extracted from this method. The values are 0.47 and 0.37 eV for 5 and 10 nm, respectively.

SAMPLES ON P-TYPE SUBSTRATES

The 5 nm sample on p-type shows higher reverse current than that for the n-type samples, while reduced reverse bias current is observed in the 10 nm sample resulting in significantly higher rectification. From the Schottky-Mott model the lower band gap of the aSiGe should influence these p-type samples more than the n-type ones, rendering the high reverse current in the 5 nm sample unexpected. This again points to the importance of interface defects on the junction characteristics in these samples

7.3.4 SAMPLES WITH SPUTTERED aSiC BUFFER LAYERS

Low reverse currents in the same range as that for the best aSi samples are observed in the samples with aSiC buffer layers on both n- and p-type substrates. These data are represented in Figure 40 along with CV data in Figure 41.

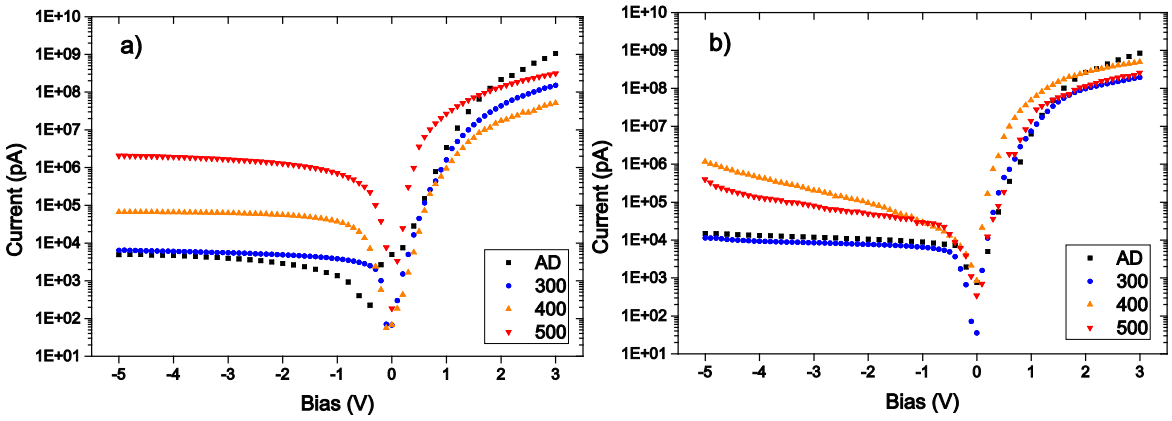

Figure 42 – IV curves from annealing experiment on samples with aSiC buffer layers of thickness 5 nm on n-type (a) and p-type (b) substrate. Only minor changes are observed from the AD sample to the 300 ℃ sample. More degradation with higher annealing temperature is observed, especially with respect to the current under reverse bias.

Samples on n-type substrates

The low reverse current is favorable for the extent of rectification, and more than five orders of magnitude are observed for both samples. The steeper forward bias region for the 5 nm sample results in an ideality factor of 1.49 and barrier height of 0.83 eV, while the corresponding values for the 10 nm sample are 2.26 and 0.91 eV.

For the 10 nm sample some irregularities at low bias can be observed. These artifacts are present for all diodes on the sample, but shape and magnitude vary. Some of the diodes on the 5 nm sample also show similar effects, although less distinct. With the high band gap of the aSiC a possible origin might be that the current is limited to tunneling of charge carriers in this region, but the measured current is close to the detection limit of the apparatus and may therefore be influenced by the measurement setup.

Similar to the previous samples the CV measurements result in higher values for the thicker buffer layers. The 5 nm sample gives a fairly linear $1/C^2$ plot resulting in a value for the barrier height at 0.51 eV. The 10 nm sample, however, deviates to some extent from linearity as seen in the $1/C^2$ plot for low reverse bias. In addition, this plot has a large slope in the linear region, giving a non-physical negative value for the built-in voltage. Different diodes investigated on this sample show some variation in slope, while the intersections with the x-axis are all at negative values.

Samples on p-type substrates

The 5 and 10 nm samples with aSiC buffer on p-type substrate are separated mainly by their different slope in the linear region. An ideality factor of 3.47 is obtained with the thinner sample, over twice as much as the value 1.52 obtained for the 10 nm sample. Despite this they give similar values for the built-in voltage and thus the barrier height at 0.80 and 0.83 eV, respectively. Barrier height values from CV data are again lower than those from IV and for these samples values of 0.54 and 0.38 eV are found for 5 and 10 nm respectively.

7.3.5 ANNEALED SAMPLES

Annealing was carried out on all samples with buffer layers deposited by sputtering. As described in detail in section 4.3 each of these samples were cut in four and annealed at 300, 400 and 500 ℃ in a forming gas flow. IV and CV measurements were carried out similarly to that of the *As Deposited* (AD) samples discussed above. In Figure 42, the resulting IV curves for samples with 5 nm aSiC buffers on both n-type and p-type substrates are shown. Minor changes are observed from the AD samples to the samples annealed at 300 ℃, while degradation becomes evident for the higher temperature anneals.

Results for the other samples are included in appendix 9.2. The same trend is not as evident as here but it may be generalized that none of the annealed samples outperform their AD counterpart, at least when it comes to rectification. An exception is the 10 nm aSiGe sample on n-type substrate, where the 300 ℃ annealing seems to improve rectification by reducing the reverse current.

As the deposition of ZnO was done at 400 ℃, the changes observed upon annealing at the same temperature was perhaps unexpected, but can be explained by the fact that sputtering is a non-equilibrium process. This non-equilibrium arises from the difference between the high energy of atoms and atom clusters incident on the substrate compared to the relatively low energy associated with the substrate temperature [87].

The choice of forming gas as the annealing atmosphere was based on hydrogen's ability to diffuse through the ZnO and contribute to passivation of dangling bonds at the interfaces and in the amorphous buffer layers. The annealing temperature in itself was also expected to contribute to the annihilation of defects and thus improvement of electrical characteristics. Since no such improvement is seen, the focus continues on the As-Deposited samples in the following investigation of junction properties.

7.3.6 SUMMARY AND DISCUSSION OF KEY PROPERTIES

Table 5 and Table 6 summarize the data for n- and p-type samples measured at room temperature presented in sections 7.3.1 through 0.

DIFFERENCE IN BARRIER HEIGHTS FROM THE DIFFERENT METHODS

In Figure 43 the barrier height values are plotted for comparison of values obtained with the different methods. The red dots represent barrier heights from IV measurements with the value for I_0 taken as the observed reverse current at $V = -5\ V$. This is done to illustrate the discrepancy between the reverse current and the one calculated from the linear region in forward bias. All samples share the trend that the calculated I_0 is smaller than the measured current in reverse bias. Thus, the reported barrier height is higher when calculating from the forward bias current. This apparent lowering of the barrier can possibly be attributed to tunneling through a narrow barrier at reverse bias. High defect concentrations at the interface can contribute in several ways enabling the tunneling mechanism. First, a high defect concentration can give a larger charge density and thus a narrower depletion region than anticipated from the depletion approximation. Second, tunneling can happen in a multistep process where several closely spaced defect levels are contributing to a hopping conductivity. [88]

Table 5 - Summary of properties for all n-type samples derived from IV and CV measurements. For the barrier heights from IV 'calc' refers to using I_0 calculated from the linear forward region, while 'readout' uses the reverse current at $V = -5\ V$.

Sample characteristics		IV data				CV data	
Buffer thickness	Buffer type	Ideality n	$\Phi_{bn}^{IV}(I_0^{calc})$	$\Phi_{bn}^{IV}(I_0^{readout})$	R_S	Built-in voltage	Φ_{bn}^{CV}
[nm]			[V]	[V]	[Ω]	[V]	[V]
0	-	1.11	0.76	0.69	600	0.33	0.60
5	aSi(PECVD)	1.99	0.66	0.54	950	0.12	0.39
10	aSi(PECVD)	1.25	0.88	0.70	900	-	-
20	aSi(PECVD)	1.33	0.87	0.77	1000	-	-
5	aSi (RT)	3.08	0.78	0.63	300	-	-
5	aSi	2.92	0.88	0.79	1800	0.28	0.55
10	aSi	1.69	0.91	0.78	450	0.15	0.42
5	aSiGe	2.13	0.80	0.70	300	0.21	0.47
10	aSiGe	4.33	0.78	0.70	1100	0.11	0.37
5	aSiC	1.49	0.83	0.77	900	0.24	0.51
10	aSiC	2.26	0.91	0.77	1200	-	-

Table 6 - Summary of properties for all p-type samples derived from IV and CV measurements.

Sample characteristics		IV data				CV data	
Buffer thickness	Buffer type	Ideality n	$\Phi_{bp}^{IV}(I_0^{calc})$	$\Phi_{bp}^{IV}(I_0^{readout})$	R_S	Built-in voltage	Φ_{bp}^{CV}
[nm]			[V]	[V]	[Ω]	[V]	[V]
0	-	2.09	0.63	0.57	4800	0.44	0.69
5	aSi(PECVD)	1.14	0.80	0.69	600	0.62	0.86
10	aSi(PECVD)	1.85	1.03	0.62	600	0.43	0.67
20	aSi(PECVD)	4.15	0.95	0.59	750	0.32	0.56
5	aSi (RT)	2.34	0.78	0.71	1000	2.18	2.42
5	aSi	2.65	0.79	0.71	1400	0.19	0.43
10	aSi	1.21	0.84	0.73	5600	0.46	0.70
5	aSiGe	2.31	0.78	0.62	1650	0.05	0.30
10	aSiGe	3.17	0.79	0.73	2000	0.50	0.75
5	aSiC	3.47	0.80	0.71	1200	0.30	0.54
10	aSiC	1.52	0.83	0.71	3000	0.14	0.38

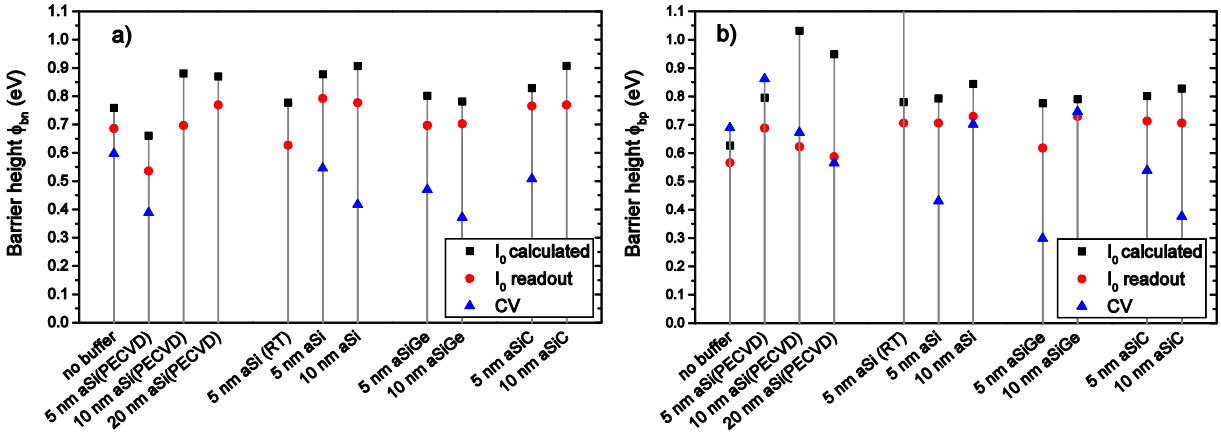

Figure 43 – Barrier heights for n-type samples as in Table 5 and p-type samples as in Table 6 are plotted in (a) and (b), respectively, for comparison of the data from IV and CV measurements.

Common to all the values derived from IV is that they are higher than what is anticipated from the Schottky-Mott model. Such high values can be described by Fermi level pinning in the heterojunction interface. Fermi level pinning is not included in the ideal models as charged defects on the interface of devices are erroneously neglected. Such charged states can pin the Fermi level and thus lead to band bending and barrier heights differing significantly from the Schottky-Mott model, even becoming completely independent on the work function and electron affinity of the materials.

Song and Guo [89] refering to Sze [18], state that Fermi pinning is common at approximately 1/3 of the band gap for Schottky junctions to n-type semiconductors. For silicon this gives a separation from the valence band of 0.37 eV for the Fermi level, and the barrier height for electrons becomes 0.74 eV. Song and Guo focus on the influence of native and thermal oxides in the ZnO/Si heterojunction. They report barrier height values of 0.79 and 0.87 eV, respectively, and attribute this to Fermi level pinning. Considering the samples in this work, the availability of defects in the interface region could be similar due to the amorphous films. Defects native to the ZnO/Si junction can also be suspected regardless of buffer as similar barrier heights are also seen by others [86, 90, 91].

Fermi pinning on the p-type samples is also possible, but as the sum of the n-type and p-type barrier heights differ from the band gap value the Fermi pinning cannot be on the same value in the band gap for both substrate types. Another possible explanation of the high barrier to p-type silicon comes from the Burstein-Moss effect, while continuing to use the Schottky-Mott model. The work function of ZnO can be described by:

$$\Phi_{ZnO} = \chi_{Si} + E_{g,Si} - \phi_{b,p} \tag{7.1}$$

as is visualized in the section 2.8 with Figure 15. Now the Burstein-Moss shift increase the band gap by occupying states in the conduction band, and a similar reduction in the work function of the ZnO can be anticipated [92]. The difference between the band gap value deduced in section 7.2.1 from the transmission measurements and the theoretical value gives the Burstein-Moss shift: $\Delta E_{F,BM} = 3.79 - 3.37 = 0.42\ eV$. The reduced work function is thus 4.23 eVimplying a barrier height to p-type Si $\phi_{b,p} = 0.94\ eV$. A more conservative shift in accordance with the literature values as discussed in section 2.8.1 is 0.28 eV when considering the non-parabolicity of the band edges. This yields a barrier

height of 0.8 eV which is in relatively good agreement with the values reported from the forward IV measurements in Table 5 and Table 6. This is also in agreement with values reported elsewhere [93].

For the n-type samples the available barrier heights from CV measurements are all lower than the two IV-derived values. Some CV data have been excluded due to unphysical, negative values for the built-in voltage. For the p-type samples the CV-derived barrier height values are more scattered, and while lower for most of the samples, some are close to or even higher than the IV values as anticipated ideally.

The fact that the CV-derived barrier heights are lower than those from IV is contrary to the expectation as was described in section 5.3. Since the slopes of the $1/C^2$ plots correspond well to the wafer specifications it is the magnitude of the whole line that is lower than anticipated from the theory. This again implies that the capacitance is higher than what theory predicts in the whole range of reverse biases. As briefly mentioned when introducing the results from the samples with PECVD buffers this may be attributed to a voltage drop outside the actual junction or a parasitic capacitance.

With the depletion approximation it is assumed that the applied voltage drop is entirely across the junction. Introducing a series resistance distorts this assumption; with Ohmic resistance there will be a voltage drop over the series resistance that is proportional to the current running through. Then the voltage across the junction is reduced by the similar amount, as described by Kirchhoff's voltage law. Considering the highest series resistance reported here for the sample without buffer on p-type, and the current running through this sample at reverse bias, the voltage drop could reach 0.06 V and provide a minor change to the $1/C^2$ plots. There is, however, no correlation between the magnitude of these quantities from IV measurements and the barrier height calculated from CV.

The alternative explanation of parasitic capacitance is considered next. Parasitic capacitance in series is ruled out as the total equivalent capacitance from two series capacitors is given by $1/C_{eq} = 1/C_{ideal} + 1/C_{parasitic}$. From this it is seen that any non-zero parasitic capacitance reduces the equivalent capacitance compared to the ideal. Parallel parasitic capacitance is the alternative that gives a possible solution. Here the equivalent capacitance is given by the sum $C_{eq} = C_{ideal} + C_{parasitic}$.

The total area of the diode is, for now, considered constant, and it is shared between the ideal and the parasitic capacitance. Referring to equation (2.31), the relation $C \propto A/W$ indicates that the parasitic capacitance must come from an area of thinner depletion region in order to increase the equivalent capacitance. Thus it is suggested that the diode is inhomogeneous with respect to depletion region thickness, and possibly charge density.

IDEALITY FACTOR

High ideality factors are seen in almost all samples in this work. Somewhat lower values are seen for the PECVD samples in accordance with this being a more gentle deposition technique, i.e. less damaging to the substrate and the interface. Otherwise there are no clear trends. Breitenstein et al. [94, 95] have attributed ideality factors $n > 2$ to recombination in extended defects such as shunts and edges for silicon solar cells. This involves mechanisms that go beyond band-to-band recombination

and trap assisted recombination. With extended defects is meant defects that are more than zero dimensional as discussed in the introductory section on defects. The result of such defects may be multiple defect levels in the band gap. Recombination through multiple trap levels can result in higher ideality factors. The amorphous buffer layers can also contribute to such a distribution of defect levels in the band gap, as has been indicated by the optical characterization of these films, and has also been investigated through DLTS as will be presented in section 7.6.

MOTIVATION FOR THE IVT AND CVT MEASUREMENTS

The validity of the Schottky-Mott model for the present samples is questioned in the above discussion, and the CV-derived values for the barrier height are indicative of inhomogeneous interface properties. Also the ideality factors are ambiguous, contesting the diode equation and the thermionic emission theory described in the introductory chapters. Thus, a clear understanding of the electronic structure and conduction mechanism is not evident from the results presented so far. This motivates further investigation of these parameters.

7.4 TEMPERATURE DEPENDENCE OF IV AND CV CHARACTERISTISCS

The continued investigation into barrier heights and ideality factors was done by looking at the temperature dependence of the IV and CV characteristics (abbreviated IVT and CVT). This was done for all the samples with sputtered buffer layers. The measurements were carried out with $40\ K$ intervals from $80\ K$ to room temperature in a liquid nitrogen cooled cryostat.

7.4.1 OBSERVATIONS FROM IVT AND CVT

Figure 44 shows the resulting curves for the IV measurements done on the samples with $5\ nm$ buffer layers of aSiC on n- and p-type substrates. The first thing to notice is the reduced current observed with lower temperatures at all biases. The noisy region in reverse bias for the low-temperature data is a result of values being out of range for the measurement equipment. For reverse bias this reduction in measured current is anticipated from the thermionic emission theory as a lower fraction of charge carriers have sufficient thermal energy to be excited across the barrier at low temperatures. A difference is seen in the temperature dependence of n-type and p-type samples; for the highest forward bias a larger reduction in the current is observed in the former than in the latter. This trend is common to all of the samples regardless of buffer type and thickness. Further, a second trend is related to the shape of the forward bias region for all samples. The linear region at low forward biases is found to have a larger slope for lower temperatures. In addition, the initial response to forward bias is observed to shift towards higher voltage as the temperature is lowered.

CV measurements for the samples with $5\ nm$ aSiC buffer are presented in Figure 45. The figure shows good linearity and fairly constant slope at all the temperatures. An increase in the built-in voltage results in increasing barrier height from the CV data as the temperature is lowered. This trend is also common for all samples.

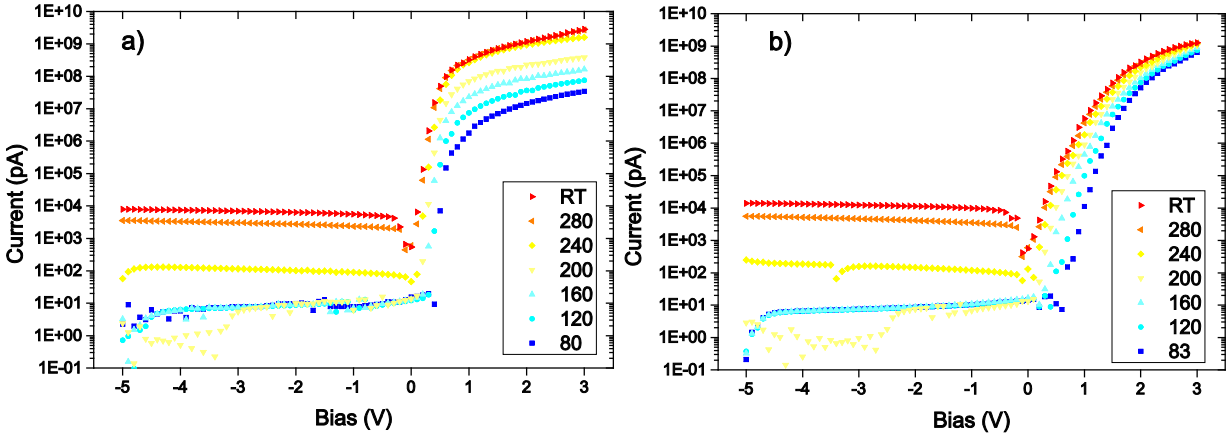

Figure 44 – Samples with 5 nm buffer layer of aSiC on n-type (a) and p-type (b) substrates. IV measurements are done in the temperature range from liquid nitrogen to room temperature, with 40 K intervals. For the low-temperature measurements the noisy curve at reverse bias is a result of values that are out of range of the measurement equipment. Plots of data from the remaining samples can be found in appendix 9.3.

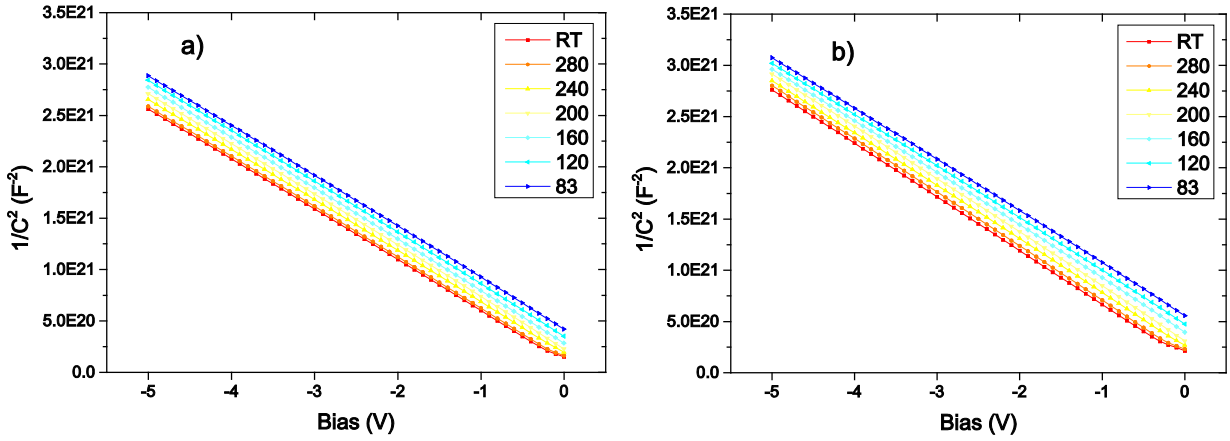

Figure 45 – CV measurements of the same samples as for IV in the previous figure. Similar figures from the remaining samples can be found in appendix 9.3.

Despite the increase in slope, the ideality factor is found to increase with lower temperature, for all samples. Thus, from the expression for the ideality, $n = q/skT$, the increase in slope does not completely accommodate the temperature change. In the n-type sample of Figure 44, the ideality goes from 1.5 at room temperature to 2.1 at 120 K. Insufficient linearity in the 80 K data precludes evaluation of the ideality from this measurement. The increase in the ideality factor is even more distinct in the p-type sample where it starts from 3.3 at room temperature to 8.5 at 80 K.

The remaining samples follow similar trends with ideality factors increasing with a factor up to three upon cooling from room temperature to 80 K. Figure 46 shows the ideality factors as function of temperature for all the measured samples on n- and p-type wafers, and the values are presented in Table 7 and Table 8.

From these measurements the samples with 10 nm buffers of aSiGe distinguish themselves with very high room temperature values. These values are significantly higher than the values obtained in the earlier measurements which can be interpreted as a sign of degradation. Such degradation might be a result of mechanical stress in the thin sputtered films.

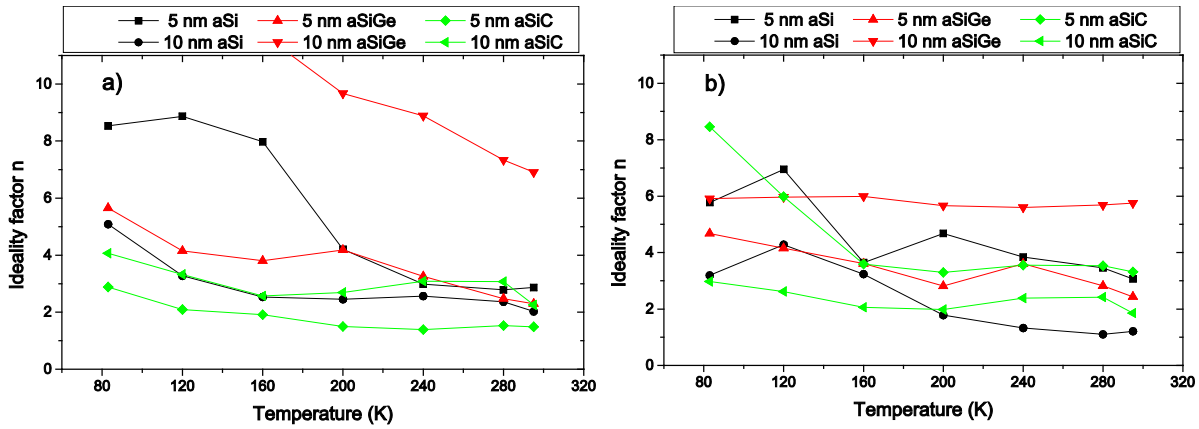

Figure 46 – Ideality factors for samples on n-type (a) and p-type (b) substrates, showing the increase upon cooling.

Table 7 - Ideality factors from IVT measurements for samples on n-type substrates.

Sample characteristics		Ideality n(T)						
Buffer thickness (nm)	Buffer type	80	120	160	200	240	260	300
5	aSi	8.5	8.9	8.0	4.2	3.0	2.8	2.9
10	aSi	5.1	3.3	2.5	2.5	2.6	2.4	2.0
5	aSiGe	5.7	4.2	3.8	4.2	3.3	2.5	2.3
10	aSiGe	20	14	11	9.7	8.9	7.3	6.9
5	aSiC	2.9	2.1	1.9	1.5	1.4	1.5	1.5
10	aSiC	4.1	3.3	2.6	2.7	3.1	3.1	2.3

Table 8 - Ideality factors from IVT measurements for samples on p-type substrates.

Sample characteristics		Ideality n(T)						
Buffer thickness (nm)	Buffer type	80	120	160	200	240	260	300
5	aSi	5.8	7.0	3.6	4.7	3.8	3.5	3.1
10	aSi	3.2	4.3	3.2	1.8	1.3	1.1	1.2
5	aSiGe	4.7	4.2	3.6	2.8	3.6	2.8	2.4
10	aSiGe	5.9	6.0	6.0	5.7	5.6	5.7	5.8
5	aSiC	8.5	6.0	3.6	3.3	3.6	3.5	3.3
10	aSiC	3.0	2.6	2.1	2.0	2.4	2.4	1.9

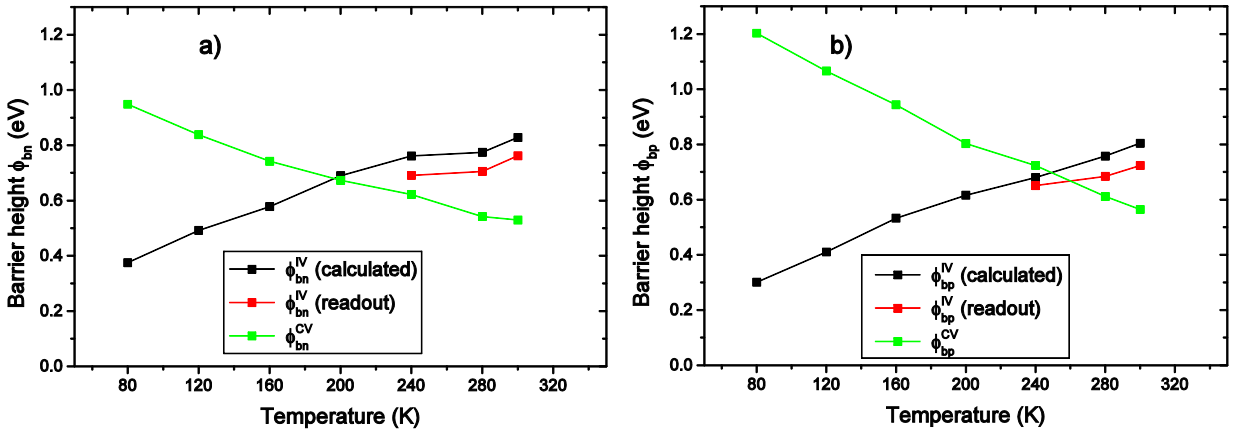

Figure 47 – For the 5 nm aSiC samples, as presented in Figure 44 and Figure 45, are here shown the barrier heights as function of temperature from the different methods used. The values of the barrier height obtained from reading the reverse current at reverse bias follow well the trend from calculated I_0 for high temperatures. For lower temperatures it is not possible to read out I_0 due to the measurements being out of range.

The barrier heights deduced from the IVT measurements are found to decrease with lowered temperature. In Figure 47 the 5 nm aSiC samples are further used as the example, and the temperature dependence of the barrier height calculated from the different measurements are plotted. Using the read out at $V = -5\ V$ still reports a lower value for the barrier height than calculation from the linear forward region for high temperatures. Temperature below $\sim 240\ K$ result in currents below the detection limit of the apparatus, as seen in Figure 44, and prevents calculation of the barrier height. The temperature dependence of the 'calculated' and 'readout' barriers seems however to be quite close. The CV-derived barrier heights are found to depend oppositely on the sample temperature, with increasing values for lowered temperature. Thus, the trend observed at room temperature, with CV values lower than IV values, is inverted at low temperatures.

7.5 Discussion of temperature dependencies

The IVT and CVT measurements supplement the room temperature measurements with further indications of samples not acting in accordance with the thermionic emission theory and the Schottky-Mott model. Different temperature dependencies are discussed in the present section, and some models are introduced in an attempt to explain the mechanisms.

7.5.1 Indications of barrier inhomogeneity

Figure 44a reveals a parallel shift of the currents to lower values for the n-type sample with 5 nm aSiC buffer at reduced temperature. Similar temperature dependence is seen also in the remaining n-type samples. An increased Ohmic series resistance cannot explain this as it would influence the curve more for higher currents. A temperature dependence of the effective barrier height is considered as a more likely explanation. This can be related to barrier inhomogeneity that has already been suggested in relation to the CV measurements. As a simplified model consider a diode with two different regions with different barrier height. One can then suggest a temperature dependence of effective area of the regions. If region one has a lower barrier height the current will

preferentially flow through this region. If then the effective area of region one is reduced with decreased temperature while maintaining the current density, the total current could be reduced without necessarily altering the barrier height.

Less influence of the temperature is seen in the forward bias region for the p-type samples, and the shift is not as parallel as for n-type samples. Similar considerations of changing the effective area can be applied to the p-type samples, as no mechanism has been suggested for this behavior for either n-type or p-type. It can be argued that the difference comes from different interaction with conduction- and valence band for the phenomenon causing the decrease in effective area.

From the CV measurements a parallel shift is seen in the $1/C^2$ plots in Figure 45. This comes from an overall reduction in the capacitance and result in higher barrier heights with decreased temperature. As the capacitance is proportional to the area of the device, the considerations of effective area can be pursued also for these data. If region one with low barrier is reduced in area as above, region two with higher barrier height might increase similarly. Contrary to IV where the low barrier region dominates the current flow and thus the measured data, CV measurements depend on the area distribution of the diode properties. If two regions coexist, the properties of the larger region will dominate. [96]

7.5.2 VARIATION IN BARRIER HEIGHT

Consider the IV data again; the barrier heights are deduced from the expression of the reverse saturation current in the diode equation:

$$\phi_{bn,bp}^{IV} = kT \ln \frac{A^* A T^2}{I_0} \tag{7.2}$$

As the barrier height is ideally a property determined by the work function and electron affinity of the two materials, it is not anticipated to have large temperature dependency. The temperature dependence suggested by the T-terms in equation (7.2) should then be cancelled by the temperature dependence of I_0. This anticipated reduction in I_0 is related to the lower thermal energy of the charge carriers, and thus reduced ability to overcome the barrier. Instead a temperature dependence is seen that implies a reduction in I_0 becoming much smaller than expected.

Svensson [97] has described temperature dependence in Schottky diodes of Cu on Si substrates. With n-type Si the temperature dependence of the barrier height corresponds to that of the Si band gap. The p-type samples show negligible variation in the barrier height. From this it is suggested that the Fermi level at the interface is pinned relative to the valence band.

In the present work, however, a temperature dependence of the barrier height is observed on both n-type and p-type wafers, and with magnitude significantly larger than the band gap changes. Therefore, the notion of Fermi level pinning relative to a band edge is not valid here. This does not exclude that Fermi level pinning occurs, but only that the pinning is not constant relative to one of the band edges.

7.5.3 Gaussian distribution of barrier heights

For IVT characteristics, a similar decrease of barrier height and increase in ideality with lowered temperature as found here is seen in several materials systems, and in this subsection some explanations are considered.

A temperature dependent ideality was first implemented by Padovani and Sumner [98] on the form of adding a constant T_0 in the expression for the reverse saturation current;

$$I_0 = A^* A T^2 \, e^{-\frac{\phi_{bn,p}}{k(T+T_0)}}. \quad \textbf{(7.3)}$$

This fits an increase in ideality factor with decreased temperature, although no physical explanation was provided. According to Sharma [99] this effect also accommodates decreasing barrier height with decreasing temperature, and can be explained by several mechanisms, including barrier inhomogeneity, tunneling and/or recombination mechanisms in competition with the regular thermionic emission.

Werner and Güttler [96] motivate the introduction of T_0 with a Gaussian distribution of barrier heights. Using the value for the barrier height obtained from CV measurements as the mean barrier height, they achieve agreement between the Gaussian distribution and their PtSi/Si Schottky diodes.

For the samples in this work, the CV-derived barrier height values are generally lower than those from IV measurements, precluding quantitative fitting with a Gaussian distribution. Although it can be argued that there are some qualitative agreement with the model in ref. [96].

7.6 Results from Deep Level Transient Spectroscopy

The presence of electrically active defects at a junction interface can be detrimental to the device performance, as concluded from the CV and IV measurements of the HIT cell structure with various buffer layers. Deep levels were introduced in section 2.3.4, and the study of these through DLTS expanded on in section 5.4. Here, the results on deep level defects at the interface, as measured by DLTS, are presented and discussed.

7.6.1 Localization of defects

To verify the spatial localization of the defects studied with the DLTS experiments, three different measurements were performed with different reverse bias and pulsing conditions. To probe interface defects a reverse bias of $V = -2\ V$ was used with pulses of $V_p = 4\ V$, i.e. a forward bias was maintained during the filling sequence (the value of V_p is relative to the reverse bias). Here, one can expect that all defects at or near the interface are filled by the pulse and thus contribute to the capacitance transients.

Using a reverse bias of $V = -5\ V$ and pulses of $V_p = 5\ V$ the depletion region from the built-in voltage remains during the pulse and defects in this region close to the interface do not contribute to the transients. With the same reverse bias and even lower pulsing at $V = 4.5\ V$ a larger region close

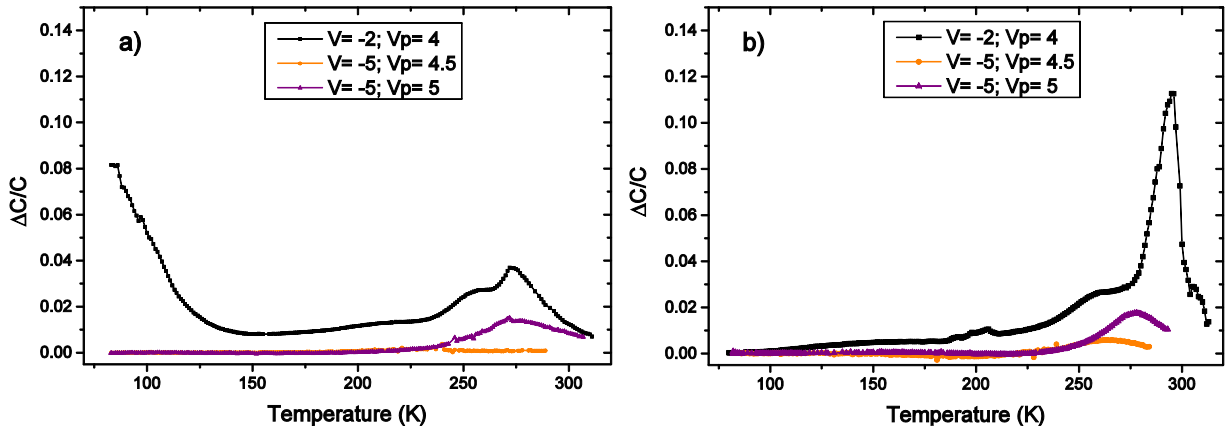

Figure 48 – 10 nm buffer layer of sputtered aSi on n-type (a) and p-type (b) wafers. The sixth window of DLTS measurements with different biasing and pulsing are shown for each sample. With reverse bias $V = -2\ V$ and pulsing with $V_p = 4\ V$ the depletion region is completely quenched during the pulse, and the interface defects contribute to the signal. With the other biasing and pulsing values the influence of interface is strongly suppressed, proving that the defects in the first measurement are actually associated with the interface.

to the interface is excluded from the measurements. The reverse bias of $V = -0.5\ V$ during the pulse corresponds to an increase in depletion length of approximately $1\ \mu m$; the effect being that only the bulk silicon is investigated.

These three biasing and pulsing settings were used on the n- and p-type samples with sputtered $10\ nm$ aSi buffers and the DLTS signal from the sixth rate window, $(640\ ms)^{-1}$, of each measurement is shown in Figure 48. It is evident that the defects are indeed located in the interface region, as they only appear in the DLTS spectra when forward bias is introduced during the filling sequence. In the following, only the first biasing option with forward injection pulsing will be used on the remaining samples.

7.6.2 Interface studies of PECVD aSi samples

Figure 49 shows the DLTS spectra of the samples with PECVD buffer layers, on n-type and p-type wafers.

For the n-type samples, DLTS peaks are observed in the low temperature region. These peaks correspond to levels that are close to the conduction band edge. Energy separation from the conduction band is in the range of 0.05 to 0.1 eV, but the broad DLTS signature is a sign of multiple overlapping levels which preclude precise determination of a unique energy position and capture cross section. As the amplitude of the peaks is proportional to the defect concentration it can be seen that all the buffer thicknesses reduce the concentration compared to the sample without buffer. The $5\ nm$ sample distinguishes itself by strongly reducing the low-temperature peak. Further, a significant baseline 'offset' is seen for all the samples with buffer, higher than that without buffer. This is indicative of widely distributed defect levels throughout the measured part of the band gap. In the $5\ nm$ sample this was anticipated from the high reverse saturation current seen in the IV measurements. However, this is less distinct with the other buffer thicknesses showing equally high 'offsets' here.

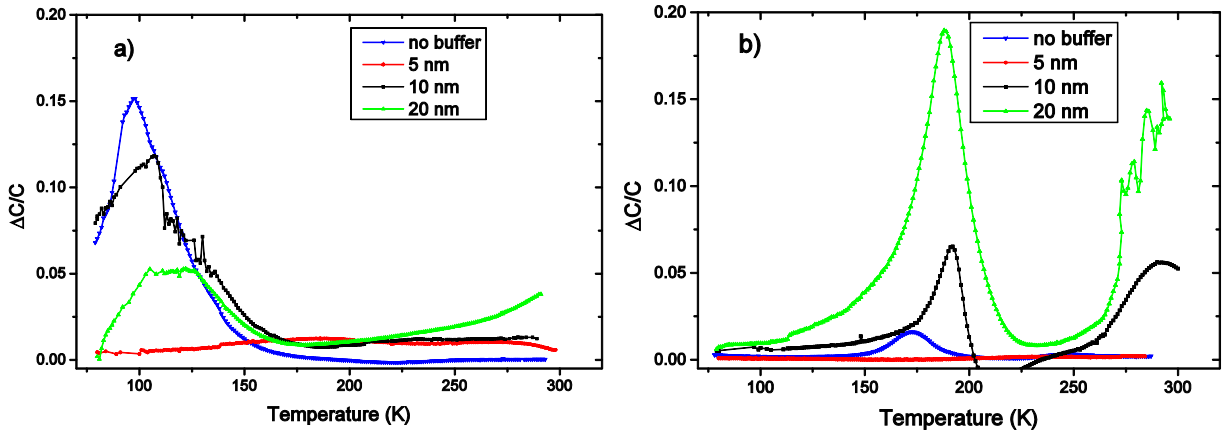

Figure 49 – The DLTS measurements of the samples with PECVD buffer on n-type (a) and p-type (b) substrates are shown.

Using p-type substrate, it is defect levels in the lower half of the band gap that are investigated. The low temperature region corresponds to levels close to the valence band, while the higher temperature peaks describes levels deeper into the band gap. For the 10 and 20 nm buffer samples, and the sample without buffer a peak is seen below 200 K. For the sample without buffer this spectrum is also shown in Figure 50a, together with those for all six rate windows used. The Arrhenius plot corresponding to these peaks as described by equation (5.29) is shown in Figure 50b. The linear fit of this plot reveals that the enthalpy of ionization is 0.38 eV above the valence band edge. The apparent capture cross section is $7.9 * 10^{-15}\ cm^2$. From the magnitude of the peak the concentration is found relative to the doping concentration by using equations (5.30) and (5.31):

$$N_t = 2N_a \frac{\Delta C_0}{C_p(\infty)} \tag{7.4}$$

This is done for all the windows, and the trap concentration is estimated from the average of these. For the 0.38 eV level the concentration corresponds to ~3 % of the doping concentration, that is $\sim 3 * 10^{13}\ cm^{-3}$ for a doping concentration of $10^{15}\ cm^{-3}$. The energy of this deep level correspond well with a value reported by Quemener et al. [48], although the capture cross section reported here is an order of magnitude smaller. A similar investigation of the peak in the 20 nm sample resulted in the values summarized in Table 9. The large magnitude of the DLTS peak of the 0.31 eV level in the 20 nm sample gives a trap concentration of 38 % of the doping concentration. Such a high value may distort the total charge density in the depletion region of the junction, and influence the capacitance by a deviation from an exponential dependence on time. For the 10 nm sample a similar peak is seen and assumed to be of the same origin, although credible values for this is hindered by the non-ideal shape of the peak.

Further broad peaks appear in the near room temperature region for 10 and 20 nm samples. These indicate significant concentrations of distributed defect levels close to the middle of the band gap. As the peaks from the other windows are out of the measurement range no trap signature values can be derived.

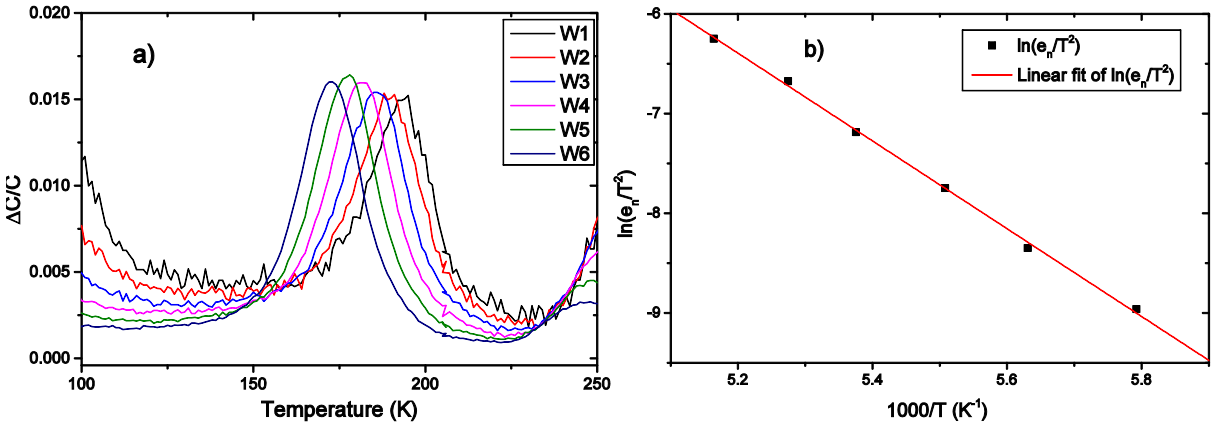

Figure 50 – This figure shows the DLTS spectrums of the sample without buffer on p-type substrate for all the six windows (a). To the right (b) is the Arrhenius plot obtained from these peaks.

Table 9 - Characterization of peaks close to 200 K **for the p-type samples without buffer, and with 20 nm aSi buffer deposited with PECVD.**

Sample	$\Delta H\ [eV]$	$\sigma_{na}\ [cm^2]$	$N_t\ [cm^{-3}]$
No buffer	0.38	$7.9 * 10^{-15}$	$3.2 * 10^{13}$
20 nm	0.31	$1.4 * 10^{-17}$	$3.8 * 10^{14}$

7.6.3 INTERFACE STUDIES OF SPUTTERED aSi SAMPLES

DLTS spectra for the sputtered aSi samples are shown in Figure 51. A significant baseline 'offset' is observed for all the samples compared to the PECVD buffers in Figure 49. This is in accordance with the expectation from the less gentle deposition technique of sputtering, and also the trend seen in the ideality factors from the IV measurements.

N-TYPE SAMPLES

For the n-type samples, Figure 51a, the high concentration seen in the sample deposited at room temperature is consistent with the high reverse current recorded for this sample. With the peak corresponding to trap concentration of almost 15 % of the doping concentration this can also be a contribution to the high capacitance seen to result in a negative built-in voltage for this sample. The Arrhenius plot for this peak indicates an energy level of about 0.3 eV and apparent capture cross section on the order of $10^{-19}\ cm^2$. The larger width of this peak compared to those analyzed above is, however, a limitation to the accuracy of these values.

Both the other n-type samples show peaks in the high temperature range. For the 5 nm sample this is disturbed by the rapid increase seen at the end of the range, so again derivation of values is precluded. The 10 nm sample seems to have contribution from two levels in this range. The lower shoulder on the peak is lost in the other windows, while the major peak seems to indicate a level close to the middle of the band gap with an energy position of ~0.5 eV bellow the conduction band. An apparent capture cross section of the order of $10^{-17}\ cm^2$ is associated with this level. In the low temperature region the signal from the 10 nm sample rise, as also seen in the PECVD sample. Although the sixth

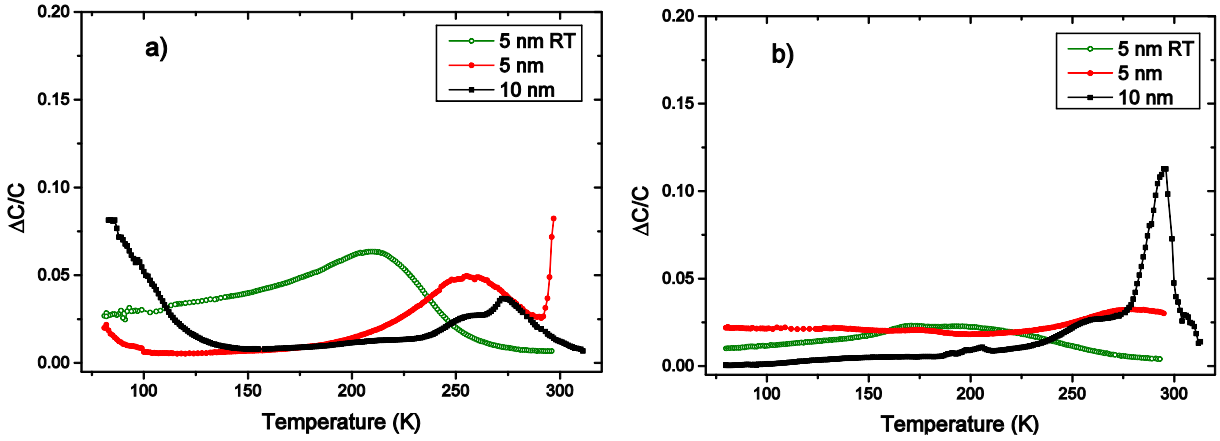

Figure 51 – DLTS signal from the sixth window is shown for samples with sputtered aSi buffer on n-type (a) and p-type (b) substrates.

window doesn't show a clear peak the other windows indicate that this is related to a defect level approximately 0.05 eV from the conduction band.

P-TYPE SAMPLES

No single defect level is apparent in the p-type samples either (Figure 51b). In accordance with the PECVD sample, the 10 nm sample here also shows sign of significant concentrations of distributed levels close to mid-band gap. It can in fact be argued that a correlation exists between the n-type and p-type samples with respect to these mid-gap level distributions.

7.6.4 INTERFACE STUDIES OF SPUTTERED aSiGe SAMPLES

Figure 52 shows the DLTS spectra for samples with aSiGe buffers on n-type (a) and p-type(b) substrates. Also the spectra from the aSiGe samples bear witness of distributed defects with energy levels covering the band gap. For the 5 nm sample on n-type substrate the peak at around 250 K indicates a trap level with a separation of approximately 0.3 eV below the conduction band edge and apparent capture cross section in the 10^{-20} cm^2 range. A similarly positioned peak in the spectrum for the p-type sample is fairly well defined, although wide, and indicates an enthalpy of 0.36 eV relative to the valence band edge and an apparent capture cross section of $4 * 10^{-19}$ cm^2. The 10 nm sample on p-type substrate shows no sign of the high mid-gap concentration seen in the aSi sample above.

7.6.5 INTERFACE STUDIES OF SPUTTERED aSiC SAMPLES

Figure 53 shows the spectra from the aSiC samples. With high-temperature peaks for the 10 nm samples these spectra resemble those from aSi. Note that the values on the y-axis are different, i.e. higher, than those of the previous buffer layers to accommodate the large peak in the 10 nm p-type sample.

N-TYPE SUBSTRATES

The 5 nm sample has a peak towards the low temperatures and in the same energy range seen for the other types of buffer layers. The range is 0.05 to 0.1 eV, but poor linearity in Arrhenius plots again

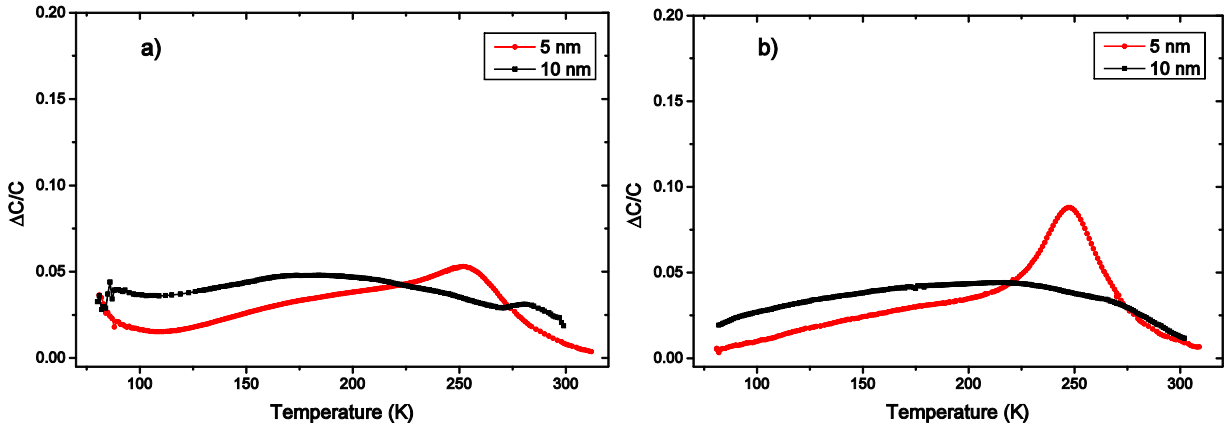

Figure 52 – Samples with sputtered aSiGe buffer on n-type (a) and p-type (b) substrates are shown.

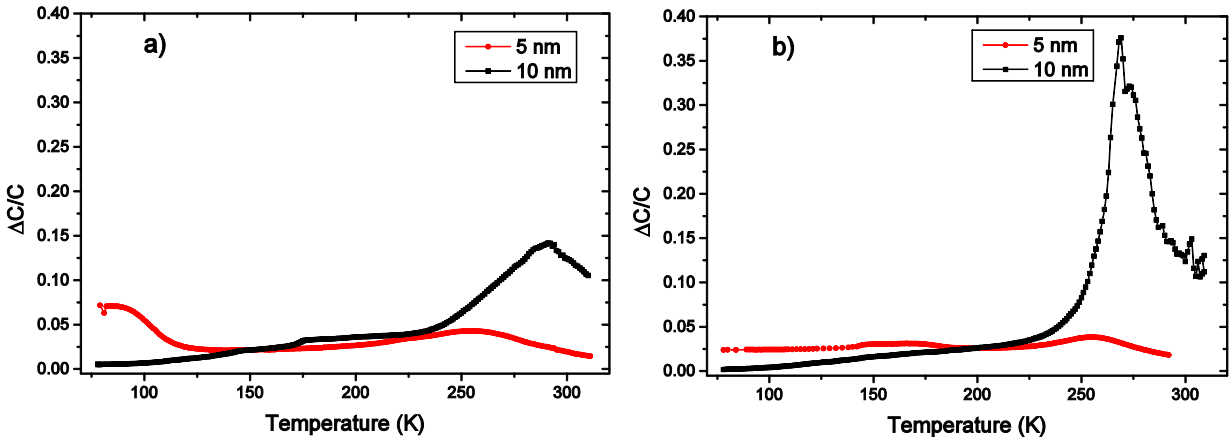

Figure 53 – Samples with sputtered aSiC buffer on n-type (a) and p-type (b) substrates are shown. Notice the higher values on the y-axis for these samples due to the high peak in the 10 nm sample on p-type.

makes an exact determination of this level difficult. Another peak, whose visibility in the figure suffers from the large y-axis values, is found just above $250\ K$ and correspond to a level $\sim 0.3\ eV$ with apparent capture cross section of $10^{-20}\ cm^2$, this is consistent with the values found in both the aSi and aSiGe samples above for the same thickness and substrate. As the major peak seen in the spectrum of the $10\ nm$ sample shifts to high temperatures (outside the range of the setup) for the shorter rate windows, it cannot be characterized regarding position and capture cross section from this data.

P-TYPE SUBSTRATES

In the $5\ nm$ p-type sample the small peak around $250\ K$ seems to be related to the $H(0.38)$ hole trap. The other signature around $150\ K$ is wider and probably a result of multiple levels. Also here a determination of reliable signature values for the major peak in the spectrum of the $10\ nm$ sample is outside the capability of the setup.

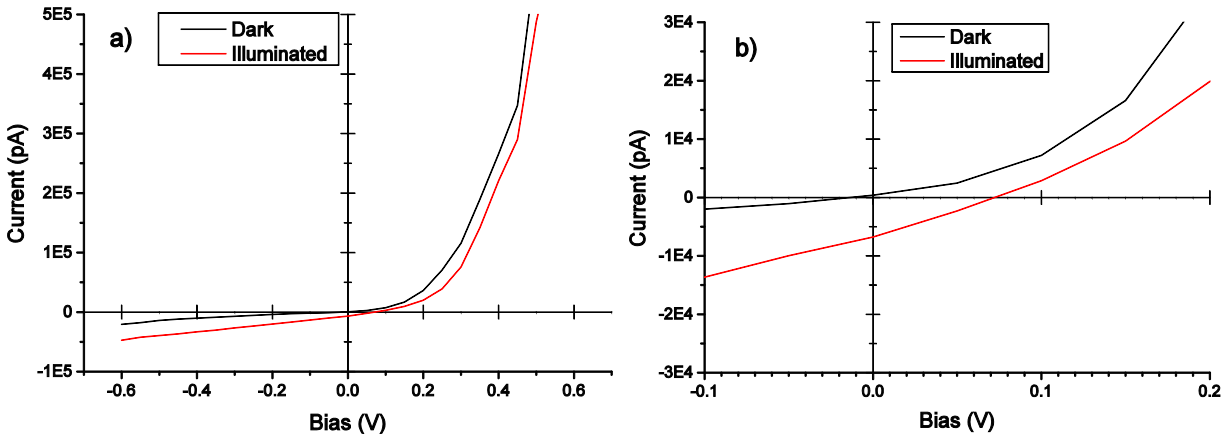

Figure 54 – Linear IV plots obtained in darkness and illumination for the sample with 5 nm thick buffer layer of aSiC on p-type substrate (a). In (b) the same plot is enhanced for visualization of power production in the fourth quadrant.

7.6.6 Discussion of DLTS results

The DLTS spectra seen in the previous subsections are generally characterized with a high baseline 'offset', and broad peaks. This indicates that there are distributions of energy levels throughout the band gap in these samples. The baseline for the samples with sputtered buffers was seen to be higher than those with PECVD buffers, in accordance with the expectations considering the nature of the deposition techniques. The defects have been localized to the interface of the heterojunction, and can to some extent be related to the properties of the IV and CV characteristics. Several of the n-type samples with sputtered buffer layers show a defect level at $\sim 0.3\ eV$ below the conduction band, a level that can possibly be attributed to the pinning of the Fermi level in p-type samples giving rise to a barrier height close to that observed with IV measurements.

7.7 Solar simulations

For the solar simulations, samples were produced, as described in section 4.4, from the structures without buffer and the ones with 5 nm buffer layer thickness. No optimization has been done with respect to conversion efficiency, as this is outside the scope of this work. Hence, the solar simulations discussed here are merely meant as a proof of concept.

IV measurements of the present samples without illumination, reveals significantly poorer rectification than the samples investigated previously. This is attributed to the defect-rich interface, as described in the preceding sections, in combination with the much larger contact area of the present samples. The large area provides a higher probability of regions with extensive defects, and thus high recombination rates that may also limit the photovoltaic response. Only a few of the samples, particularly the ones on p-type substrate, show photovoltaic response. In Figure 54 the IV curves for the structure with 5 nm aSiC buffer on p-type substrate is depicted, as performed in darkness and under illumination. With illumination the curve is seen to shift towards lower currents, in agreement with photo-generation of charge carriers. The fourth quadrant is emphasized in Figure 54b, from this illustration it is seen that the values obtained for V_{OC} and I_{SC} are small, and no further quantification of the properties is pursued.

8 SUMMARY AND CONCLUSIONS

Heterostructures of ZnO/buffer/Si have been investigated, with buffer layer thicknesses in the $5 - 20\ nm$ range and composed of aSi, aSiGe and aSiC. Synthesis of samples with PECVD and sputter deposition was followed by characterization, with primary focus on electrical properties through IV, CV and DLTS.

The ZnO films were analyzed with Hall and transmittance measurements, where a resistivity of $1.57 * 10^{-3}\ \Omega\ cm$ and mean transmittance of 83 % in the visible range was obtained. From depositions of the buffer materials on glass substrates, XRD measurements indicate that the films are amorphous, also after heat treatment at temperatures similar to those used during the ZnO deposition. Transmittance and PL measurements of these buffer samples reveal no clearly defined band gap value, but indicate gradual onset of absorption till 3 eV.

The IV characteristics show that rectification exceeding five orders of magnitude is possible for samples on both n-type and p-type substrates. PECVD aSi buffers were seen to be a positive influence on p-type samples, with improved reverse current and rectification for thinner buffers. Increased ideality factor was found for samples with sputtered buffers compared to PECVD, in accordance with the expectations. Evaluating the barrier height revealed large differences from IV and CV. The CV-derived values were lower than those from IV, which can possibly be attributed to inhomogeneous barriers. At the same time, the barriers obtained by IV are higher than predicted from the Schottky-Mott model, which is indicative of Fermi level pinning at interface defect states. This motivated the continued inquiry with temperature dependent IV and CV. Distinct temperature variations were observed for the barrier heights determined from both IV and CV measurements, with trends common to all samples. Decreased barrier height and increased ideality factor are found from IVT upon decreased temperature, this is qualitatively consistent with inhomogeneous barriers as described in the literature. However, the low barrier height values extracted from CV preclude a quantitative description. CVT yields opposite temperature dependence for the barrier height, and it is suggested that the effective area of different regions in the junctions depend on the temperature. Interface defects were investigated with DLTS, and although some peaks were seen and analyzed, the general tendency is a relatively high concentration of distributed levels throughout the band gap.

The variation of the rectifying properties with varying the buffer composition is low, but with one possible exception of the aSiGe samples on n-type substrates, where slightly lower reverse current is observed. It is, however, difficult to relate this lowered reverse current to results from the other experiments. The lower band gap of aSiGe compared to the other buffer materials might contribute to a lower barrier. But contrary to the assumptions in the simulations, the electron affinity of aSiGe would have to be greater than that of Si for a reduced barrier to n-type substrates. Different electron affinity than that used in the simulation cannot, however, be excluded as the literature values vary. A possible explanation for the lack of variation between the samples with different buffer composition is again Fermi level pinning. Hence, the strong influence of defects supersedes the dependence on the

work function and electron affinity. With a wide distribution of defects from the Si/ZnO interface as a base it can be argued that the Ge and C contributions in the reported samples are minor.

The large interface defect concentrations are also suggested to contribute to recombination of photo-generated charge carriers, and thus limit the photovoltaic response.

8.1 SUGGESTIONS FOR FURTHER WORK

Although XRD performed on buffer material deposited on glass shows no crystallinity, Metal Induced Crystallization (MIC) can occur in the heterostructure. A Transmission Electron Microscopy (TEM) study of the interface would be interesting to determine if this is the case. Atomic force microscopy could be utilized to investigate the thickness homogeneity of the buffer thin films. To do so, deposition of the relevant thicknesses must be done on Si wafers, as rough glass substrates or thicker films would distort the accuracy.

Other suggested actions involve different deposition techniques. The compositional variations have been found to give limited influence on the sample properties. Larger variations are seen in the literature with different deposition techniques used to synthesize only the ZnO/Si structure without buffer. More gentle techniques such as Atomic Layer Deposition (ALD) yield results closer to the ideal models, as the surface is less prone to be damaged during the deposition. ALD of the ZnO can also be done at lower temperatures, further reducing the probability of MIC. Deposition of the buffer layers with hydrogen passivation should be considered also, to minimize dangling bonds, and thus defects in the buffer layer and on its interfaces.

Further work can also be suggested with respect to simulations. Implementation of interface defect concentrations would be interesting. So would also simulations of optical response in the structure. In this context, a more careful determination of the properties of the amorphous buffers, e.g. work function and band gap, would be favorable.

9 APPENDICES

9.1 SILVACO SIMULATIONS

9.1.1 PHYSICAL MODELS USED IN THE SIMULATIONS

fldmob is a model for field dependent mobility.
conmob uses tabulated values for concentration dependent mobility, these values are used for Si at 300 K.
srh is a model for Shockley-Read-Hall (SRH) recombination which is recombination assisted by traps in the band gap.
consrh is a SRH model where concentration dependence is accounted for, this is appropriate for Si.
fermi the whole Fermi-Dirac equation is included in this model, replacing the default Boltzmann equation, this is necessary for highly doped materials.
auger allows Auger recombination, important at high current densities.
optr is a model for band to band recombination in direct band gap materials.
bgn is a model for band gap narrowing, appropriated for highly doped regions.

qtunn.el describes tunneling of electrons through a barrier due to an insulator.
qtunn.ho as above but for holes

print is a useful command, giving real time printing of the calculated data.

THE INTERFACE STATEMENT

The parameter **s.s** indicates that the models used apply to semiconductor-semiconductor heterojunctions. **thermionic** accounts for thermionic emission across a barrier, while **tunnel** allows tunneling through the barrier. Interface recombination rates can be specified for electrons and holes with **s.n** and **s.p** with unit cm/s.

9.1.2 INPUT FILE

```
go atlas
mesh space.mult=1.5
#
x.mesh loc=-5.00 spac=1
x.mesh loc=-3.00  spac=0.05
x.mesh loc=3.00   spac=0.05
x.mesh loc=5.00  spac=1
#
y.mesh loc=0.00 spac=0.5
y.mesh loc=0.18 spac=0.5
y.mesh loc=0.19 spac=0.05
y.mesh loc=0.20 spac=0.001
y.mesh loc=0.21 spac=0.001
y.mesh loc=0.25 spac=0.005
y.mesh loc=8.00 spac=0.1
y.mesh loc=50   spac=2
#
region num=1 material=ZnO      x.min=-5  x.max=5   y.min=0.0    y.max=0.2
region num=2 material=Si       x.min=-5  x.max=5   y.min=0.2    y.max=0.21
region num=3 material=Si       x.min=-5  x.max=5   y.min=0.21   y.max=50
#
electr  name=anode     top       x.min=-3   x.max=3  material=Aluminum
electr  name=cathode   bottom    x.min=-3   x.max=3  material=Silver
#
material region=1 eg300=3.37 affinity=4.65 NC300=9e18
material region=2 eg300=1.9  affinity=4.0   mun=20  mup=1.5  nc300=2.5e20  nv300=2.5e20
material region=3 eg300=1.12 affinity=4.05
#
doping uniform   region=1   n.type concentration=1e20
doping uniform   region=2   n.type concentration=1e12
doping uniform   region=3   n.type concentration=1e15
#
interface s.s thermionic tunnel
#
model    conmob fldmob consrh auger optr bgn fermi Temp=300 qtunn.el qtunn.ho print
#
solve      init
output band.param con.band val.band recomb photogen u.srh u.auger u.radiative
#
STRUCT OUTFILE=ZnOSi_1.str
Tonyplot ZnOSi_1.str
#
method newton
#
log   outfile=ZnOSi.log
solve      vcathode=-3.0  vstep=0.2  vfinal=3.0  name=cathode
tonyplot ZnOSi.log
#
quit
```

9.2 IV OF ANNEALED SAMPLES

In the following figures the IV curves for all the annealed samples are presented, except for those shown in section 7.3.5. Samples on n-type substrates are to the left (a) and p-type to the right (b), with otherwise equal parameters in each figure.

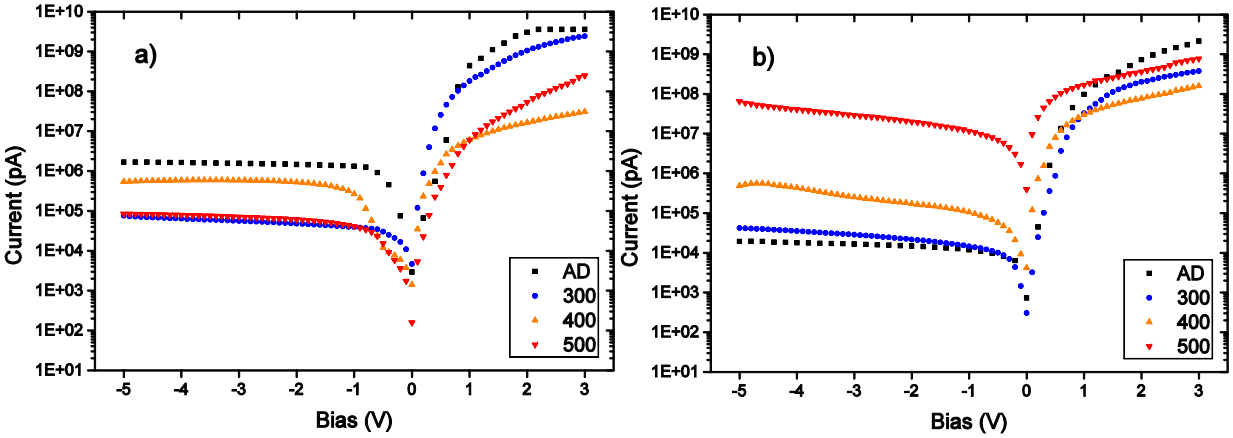

Figure 55 – Samples with 5 nm buffer layer of aSi n-type (a) and p-type (b) substrates. These are the samples made with all sputtering undertaken at room temperature.

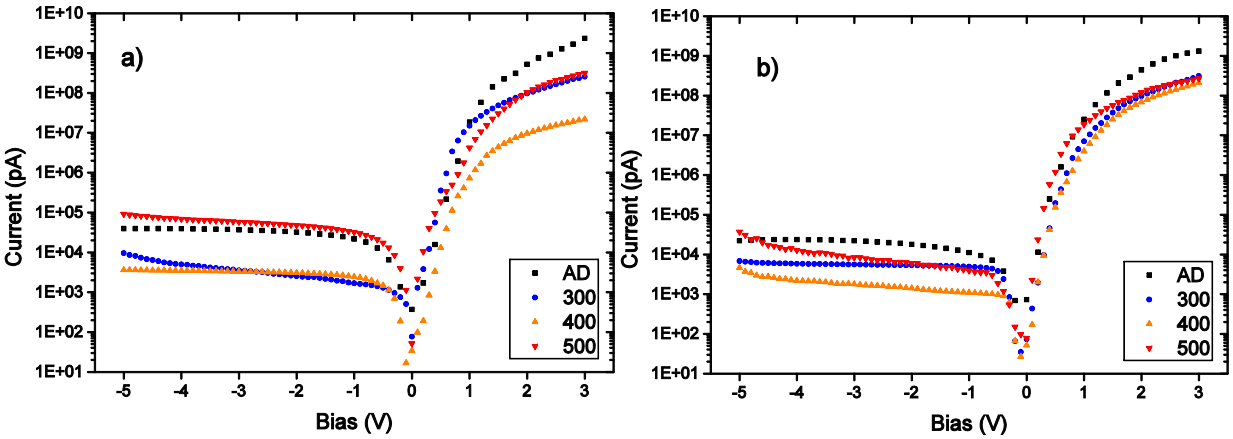

Figure 56 – Samples with 5 nm buffer of aSi, and with AZO sputtered at 400 ℃ n-type (a) and p-type (b) substrates.

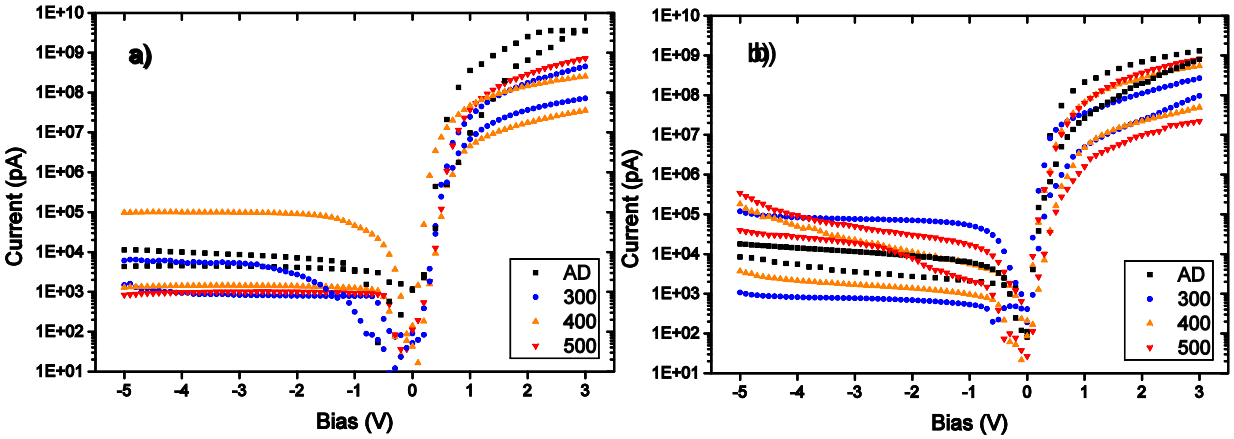

Figure 57 – Samples with 10 nm buffer layer of aSiGe n-type (a) and p-type (b) substrates.

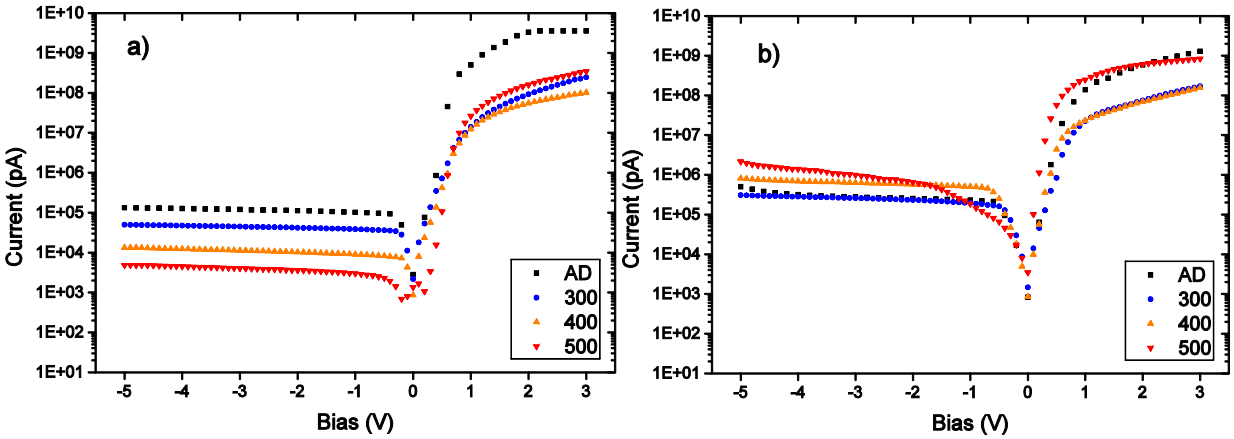

Figure 58 – Samples with 5 nm buffer layer of aSiGe n-type (a) and p-type (b) substrates.

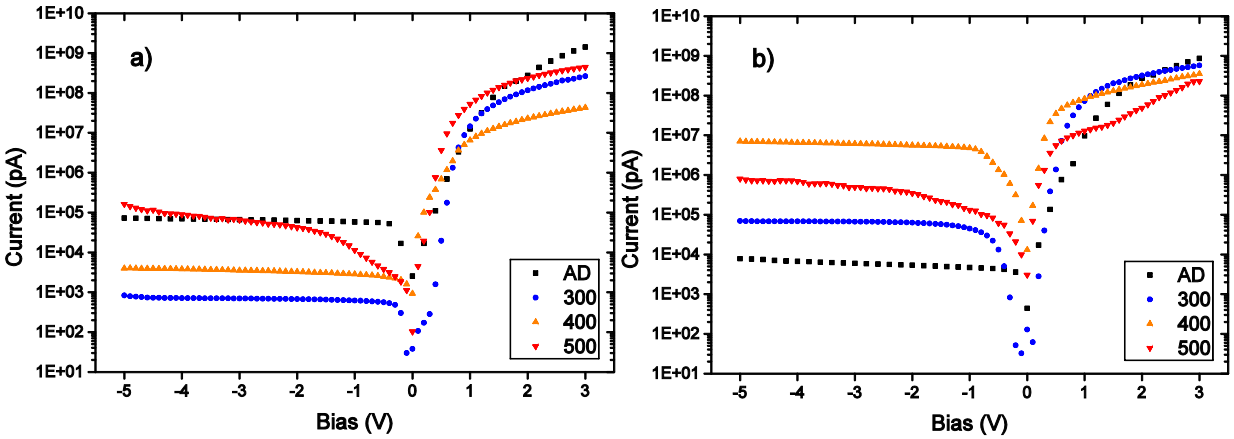

Figure 59 – Samples with 10 nm buffer layer of aSiGe n-type (a) and p-type (b) substrates.

9.3 IVT AND CVT DATA

Figures of IVT and CVT data for the remaining measured samples, not presented previously, are found here.

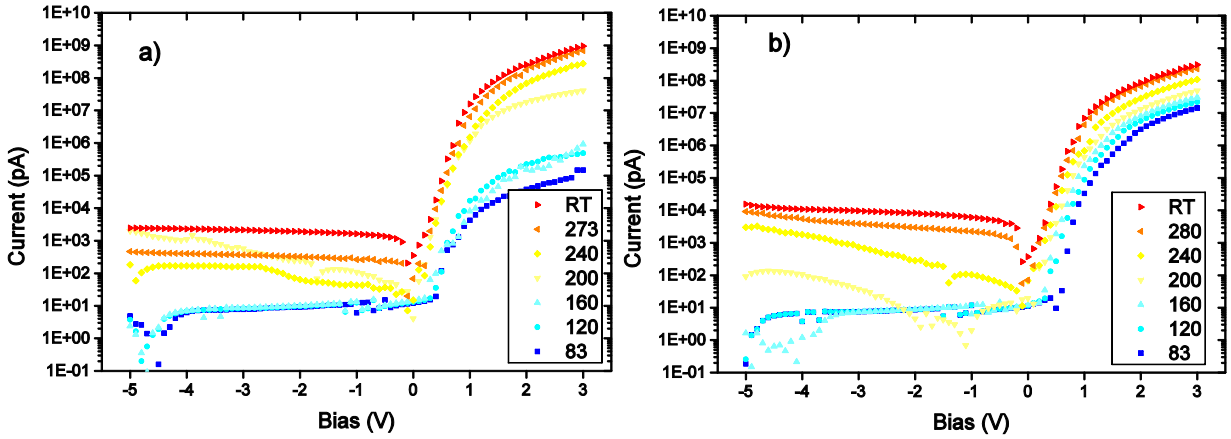

Figure 61 – Samples with 5 nm buffer of aSi, and with AZO sputtered at 400 ℃ n-type (a) and p-type (b) substrate.

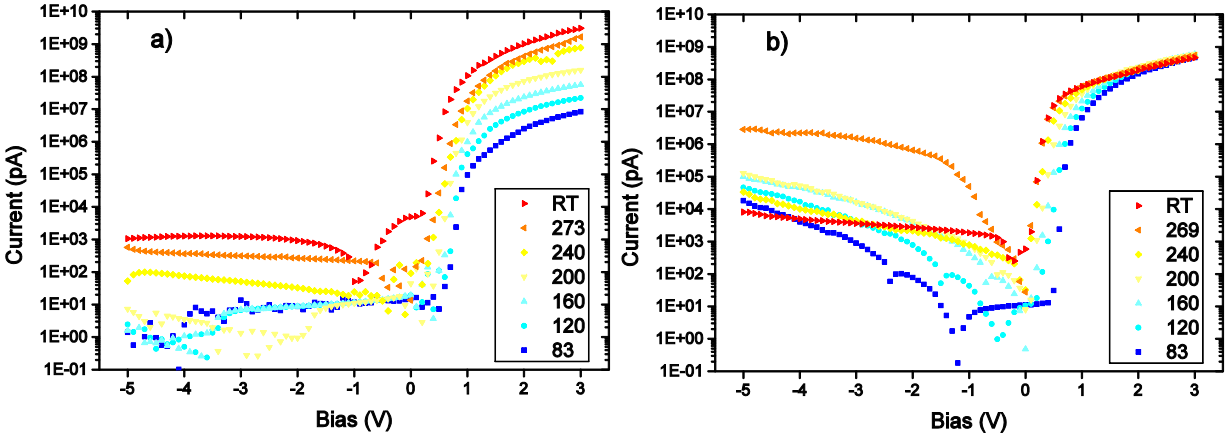

Figure 62 – Samples with 10 nm buffer layer of aSi n-type (a) and p-type (b) substrate.

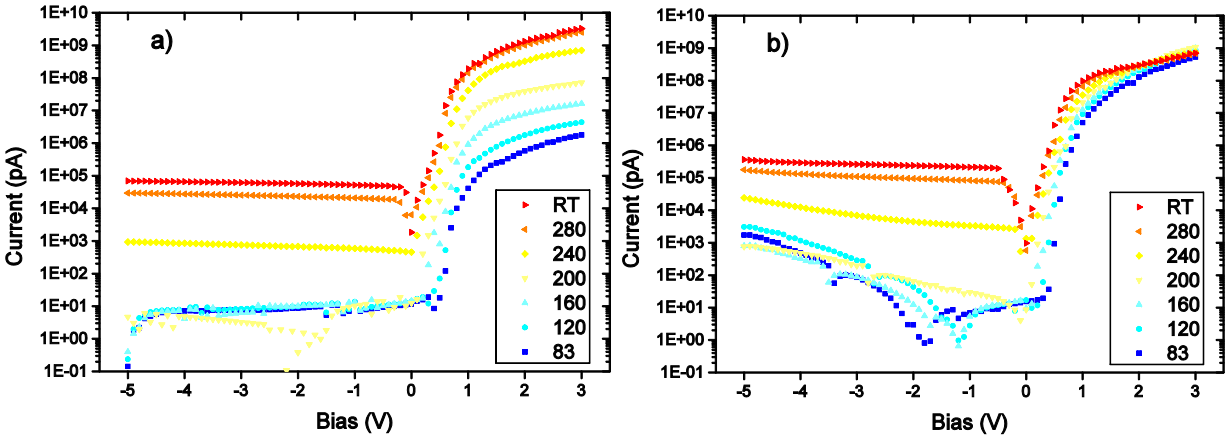

Figure 63 – Samples with 5 nm buffer layer of aSiGe n-type (a) and p-type (b) substrate.

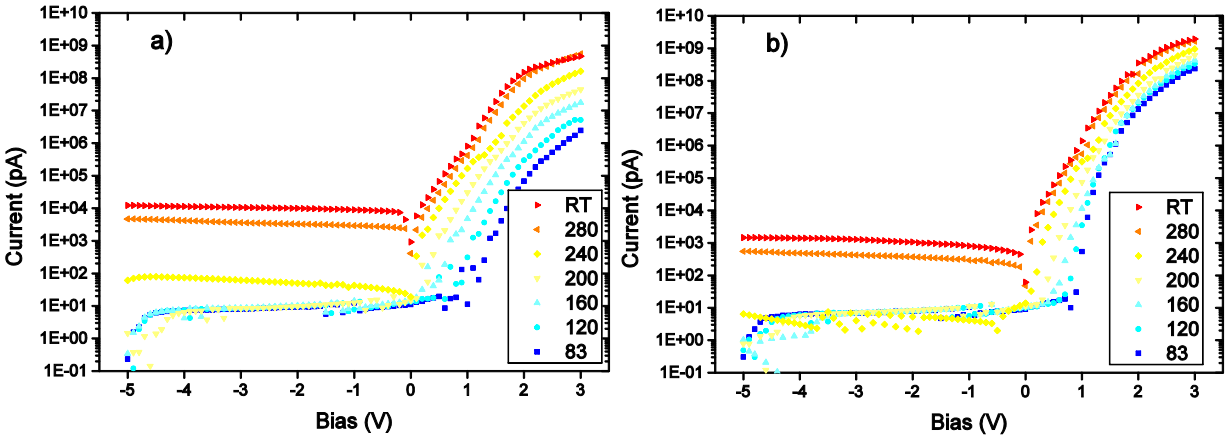

Figure 64 – Samples with 10 nm buffer layer of aSiGe n-type (a) and p-type (b) substrate.

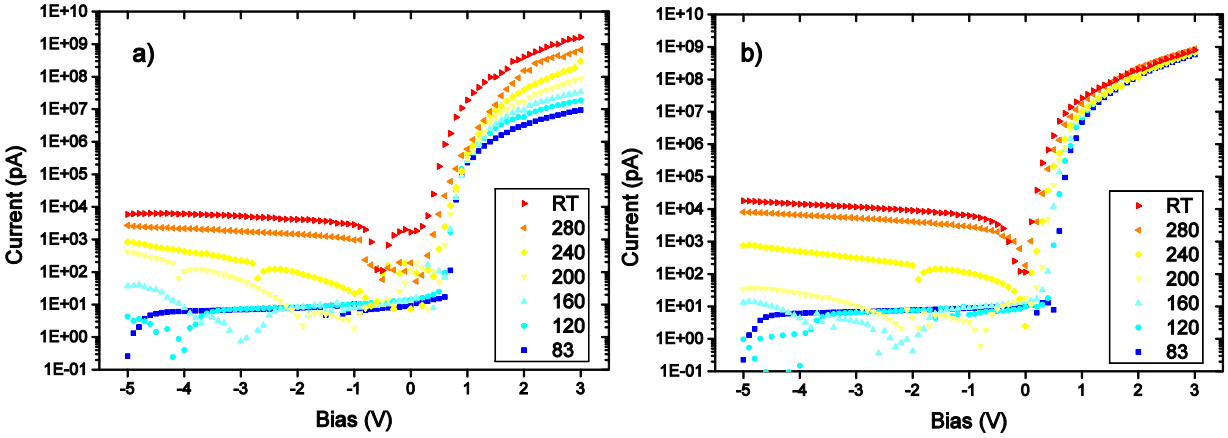

Figure 65 – Samples with 10 nm buffer layer of aSiC on n-type (a) and p-type (b) substrate.

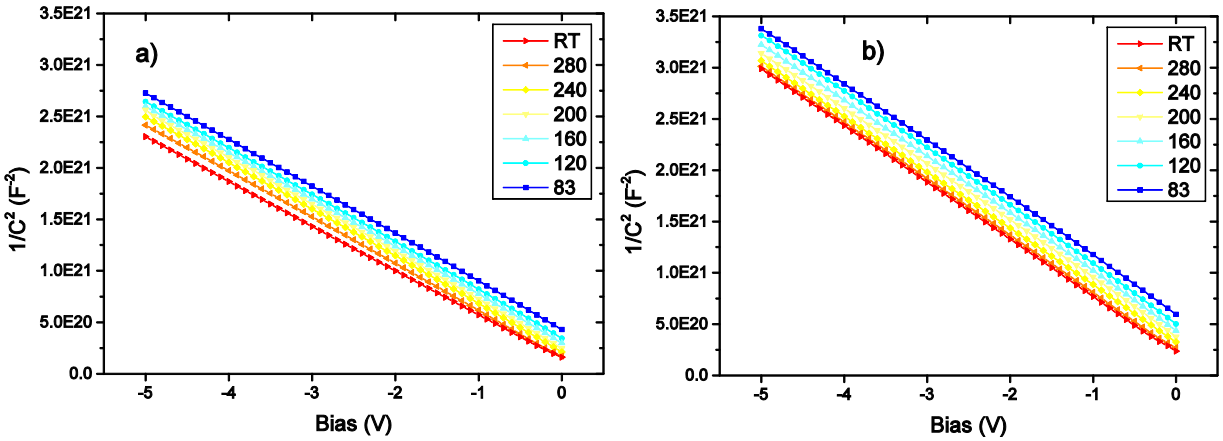

Figure 66 – CVT measurements of samples with 5 nm buffer of aSi, and with AZO sputtered at 400 ℃ n-type (a) and p-type (b) substrate.

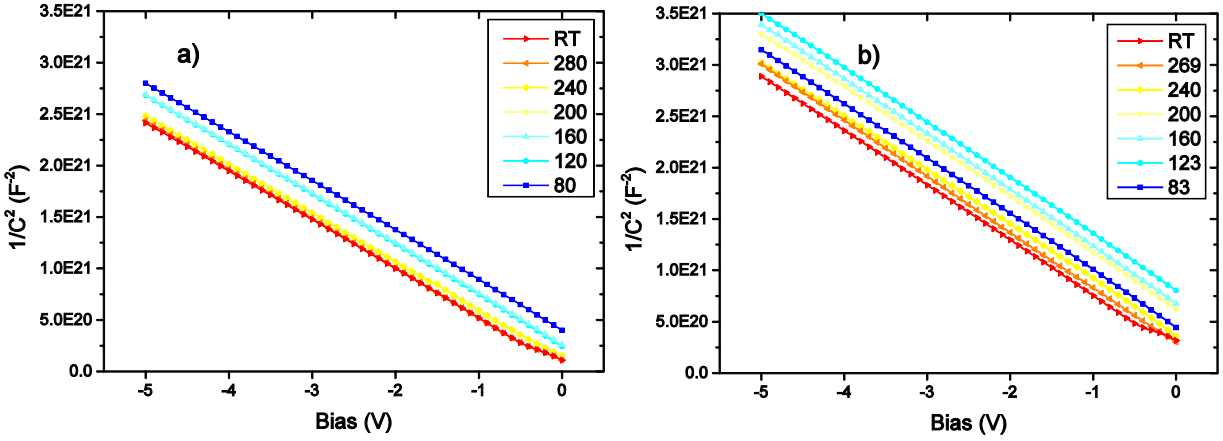

Figure 67 – CVT measurements of samples with 10 nm buffer layer of aSi n-type (a) and p-type (b) substrate.

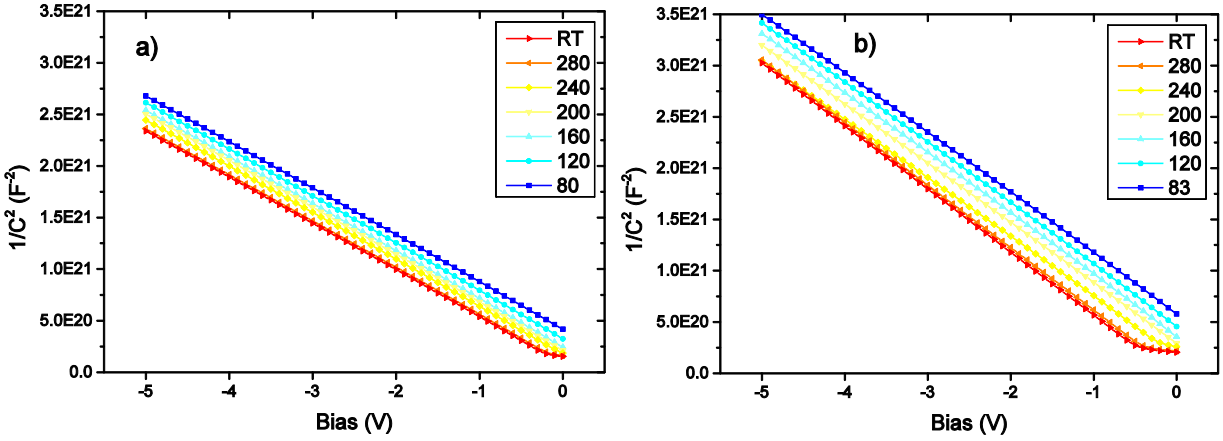

Figure 68 – CVT measurements of samples with 5 nm buffer layer of aSiGe n-type (a) and p-type (b) substrate.

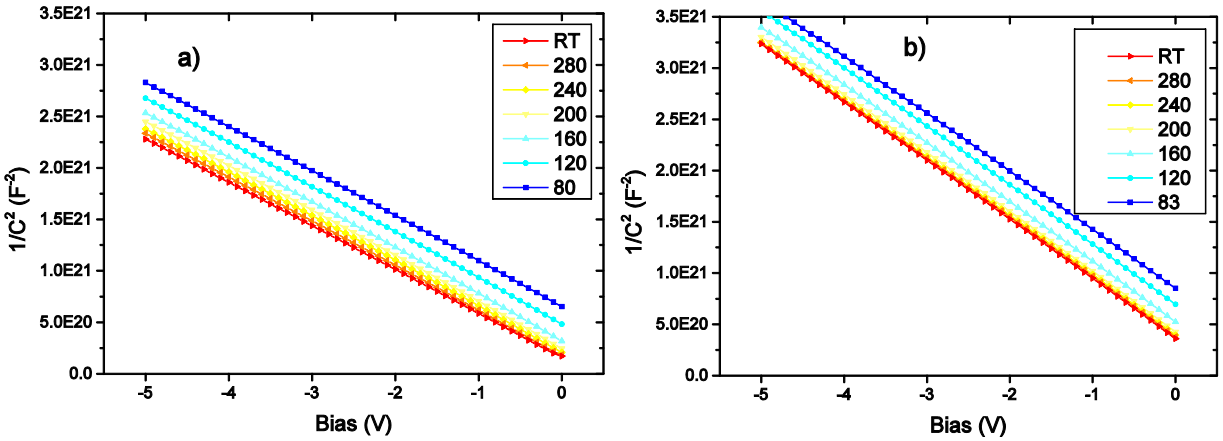

Figure 69 – CVT measurements of samples with 10 nm buffer layer of aSiGe n-type (a) and p-type (b) substrate.

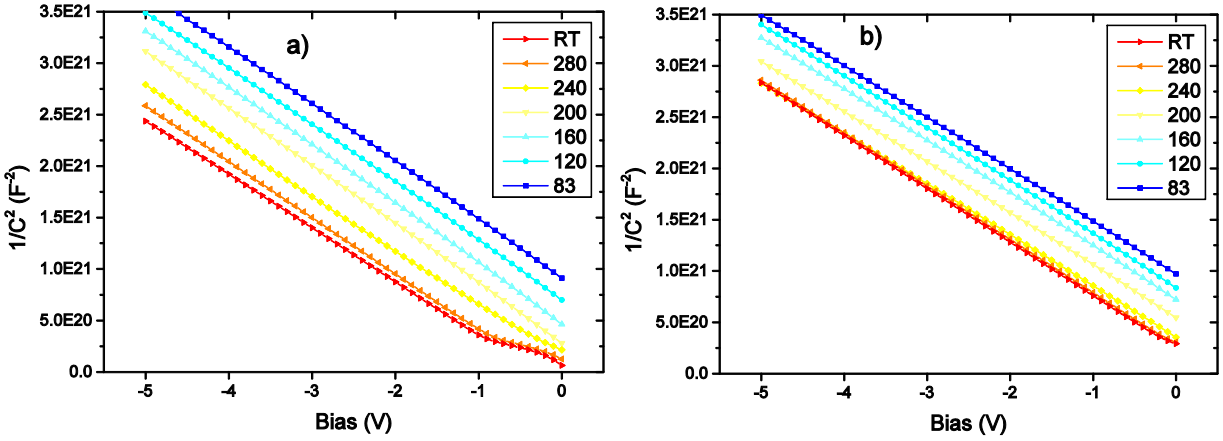

Figure 70 – CVT measurements of samples with 10 nm buffer layer of aSiC on n-type (a) and p-type (b) substrate.

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